RT Box

Tutorial

Building a Simple Voltage Source Inverter

Using just one RT Box and a D-Sub loopback cable

Tutorial Version 1.0

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1 Introduction

In this tutorial you will build a simple three-phase voltage source inverter (VSI) for deployment on the RT Box. The tutorial is oriented towards users making their first practical models for the RT Box using PLECS Standalone and identifies potential missteps ones may make along the way.

The primary learning goal for the tutorial is to demonstrate the limitations of conventional switch models in real-time applications, motivating the use of sub-cycle averaging and specialized hybrid power modules in later tutorial exercises.

Before you begin If this is your first time using the RT Box, you should complete the “Introduction to the RT Box using PLECS” tutorial prior to starting this tutorial to understand how to build and deploy basic models.

The tutorial is designed so that it can be completed with only an RT Box and a loopback cable. The loopback cables are used to drive the RT Box analog and digital inputs from the RT Box outputs. A D-SUB 37-pin male-to-female cable can be used for this purpose.

2 Building a VSI model in PLECS

In this section you will create a simple VSI model using the PLECS power modules and an open-loop PWM generator. You will then run the plant and modulator on one RT Box. Note at this point that running both plant and modulator together is not the normal approach for rapid control prototyping (RCP) or hardware-in-the-loop (HIL) simulations. In these cases the controller or the plant is deployed separately onto one RT Box and tested with the actual hardware or a controller in use. However, using just one RT Box for both still allows users with only one RT Box to see important effects like sampling resolution and execution time.

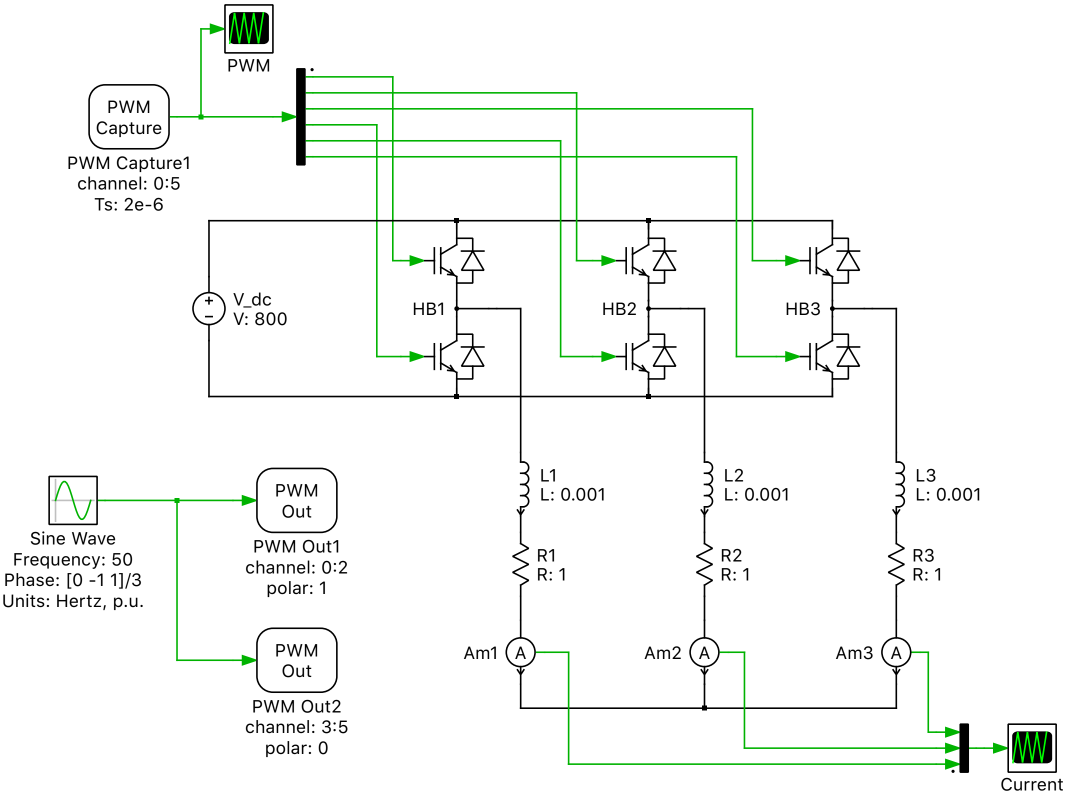

Figure 1: A simple real-time VSI model

Your Task:

1 Create a new PLECS model and build the VSI and PWM modulator given in Fig. 1. Use the Half Bridge component from the “Electrical”, “Power Modules” section of the PLECS component library. Use a PWM Capture block from the PLECS RT Box library and connect it to the IGBT gate inputs as shown in the figure. Also note the difference in the **Polarity** setting for the two PWM Out components.

Use the default component parameters unless noted differently in Fig. 1.

2 Use a DSUB loopback cable to connect the Digital Out ports on the RT Box front panel with the Digital In ports.

3 Open the **Coder options...** menu and enter a discretization step size of $5\mathrm{e}{-6}$ seconds, select your RT Box target in the **Target** tab and click **Build**.

? Connect to the External Mode and check the simulation scopes. What do you see? Is this result reasonable?

A The “PWM” Scope should show six PWM signals which are on the range of zero to one. Right click the Scope window and select **Spread signals** to view all six inputs at once. The “Current” Scope should show a balanced three-phase sinusoidal inductor current. These results are expected based on the sinusoidal input signals to the PWM Out blocks.

? What is the execution time of the model and processor loading? These performance metrics can be accessed from the RT Box Web Interface. Can the model complexity be increased?

A The average execution time of the model should be near $2.2\,\mu\mathrm{s}$ and the processor loading will be $40\,\%$ to $45\,\%$. The model complexity can be increased since the processor loading is well below $100\,\%$. Alternatively, the simulation time step could be further reduced.

After completing these tasks, your model should be the same as the reference model `vsi_loopback_1.plecs`.

3 Building a VSI model in PLECS with discrete components

In this section you will replace the half-bridge power modules with discrete IGBT components. This exercise is supposed to highlight some of the limitations of conventional (discrete) switch models in real-time applications.

Note: *Always* use the dedicated power modules when building up a converter topology for real-time simulation since using discrete components can mean high loss in simulation accuracy!

To simulate a PLECS model in real-time, the model must be discretized to run at a fixed sample time using a fixed-step solver. The ideal sample time, or discretization step size, is a compromise between system model fidelity and accuracy of the simulation results. Conventional switch model performance in real-time applications is closely coupled to the chosen discretization step size, as the switch state can only change once per simulation time step. This limits the number of achievable duty cycles within a switching period.

With conventional switch models, a comparatively small step size must be chosen relative to the PWM switching frequency to achieve acceptable model fidelity. When small time steps are chosen, there is a limited amount of time to execute the required model calculations on the CPU prior to the start of the next model time step.

Your Task:

1. Replace the half bridge power modules in Fig. 1 with discrete IGBT with Diode components that you can find in the Electrical + Power Semiconductors section of the PLECS library. Use a Digital In block from the PLECS RT Box library and connect it to the switch gate signals as shown in the figure. Keep the rest of the model the same as in Fig. 1.

2. Deploy the model on the RT Box with the same discretization step size of $5\mathrm{e}{-6}$ seconds as before.

   Connect to the External Mode and check the simulation Scopes. What do you see? Do the current measurements show any unexpected characteristics?

   The “PWM” Scope should show six PWM signals which are either zero or one. The “Current” Scope will show a balanced three-phase sinusoidal inductor current. However, you will also notice a periodic oscillation on the peak current magnitude and additional harmonic distortion compared to the results from the previous exercise. This is a consequence of the limited PWM resolution.

3. Disconnect from the External Mode and change the discretization step size to $2\mathrm{e}{-6}$ seconds. Build the model and deploy it to the RT Box. Connect to the External Mode and check the simulation Scopes.

   Do the real-time simulation results seem reasonable?

   Decreasing the discretization time step from $5\mathrm{e}{-6}$ seconds to $2\mathrm{e}{-6}$ seconds helps to improve the PWM resolution. There is a corresponding reduction in the distortion and non-ideal characteristics of the current waveform under these operating conditions.

   What is the execution time of the model and processor loading? These performance metrics can be accessed from the RT Box Web Interface. Can the model complexity be increased?

   The processor loading will be near $100\,\%$ with an execution time of $2.0\,\mu\mathrm{s}$. The model complexity cannot be further increased.

4. Disconnect from the External Mode. Add the Sine Wave Generator to the parameter inlining exceptions list. Once again, build the model and deploy it to the RT Box maintaining a discretization step size of $2\mathrm{e}{-6}$ second.

   After deploying the model and connecting via the External Mode, change the Sine Wave amplitude from 1.0 to 0.2.

   Do the real-time simulation results seem reasonable? Why is the simulation sensitive to these conditions? With a $2\mathrm{e}{-6}$ seconds discretization step size and a 10 kHz PWM signal, is there a limit to the total number of achievable switch duty cycles with a conventional switch model?

A model comprised of Discrete IGBT components will show significant non-ideal harmonics on the current waveforms at lower duty cycles. A 10 kHz PWM signal has a $100\,\mu s$ period, so with a $2.0\,\mu s$ discretization step size it is only possible to sense 50 different duty cycles. When a PWM Capture component is used the $7.5\,ns$ sampling resolution of the FPGA results in the ability to sense 13,333 different duty cycles for the same 10 kHz PWM waveform.

After completing these tasks, your model should be the same as the reference model `vsi_loopback_optional.plecs`.

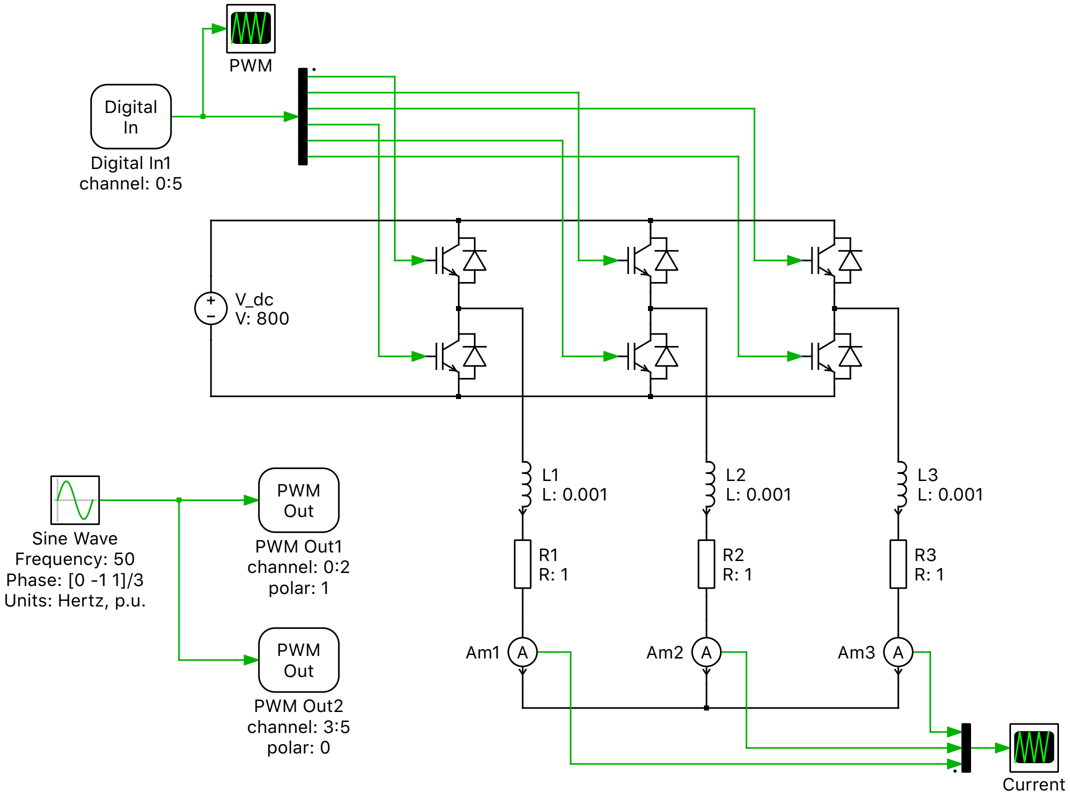

Figure 2: A simple VSI model with conventional switches

4 Conclusion

Conventional switch models have limitations in real-time applications. The switch state can only be updated once per simulation time step, requiring a relatively small discretization step size relative to the PWM period. This leads to high processor utilization even for relatively simple models and poor performance at low duty cycles.

The next several tutorial exercises will demonstrate how to overcome these modeling challenges by using sub-cycle averaging and specialized hybrid power modules.

Revision History:

Tutorial Version 1.0	First release

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