Modeling a PFC controller using PLECS®

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1 Introduction

Active power factor correction (PFC) is used extensively in AC-DC converters since it allows the converter to meet harmonic standards without the need for a bulky and costly input filter that normally accompanies a passive AC-DC converter. In this application note, a single-phase boost-type 600 W PFC converter is modeled in PLECS. The schematic of the example PFC converter is given in Fig. 1 and the key parameters of the converter are given in Table 1. The controller, based on a typical commercially-available PFC control IC, is modeled as a custom component and includes features such as interleaved switching and frequency dithering. A design procedure for the current and voltage controllers using PLECS Analysis Tools is also given. The open-loop small-signal Bode plots of the current and voltage loops are first obtained, allowing the controllers to be designed and the loop gain to be predicted. Example model files accompany this application note, and are described in Appendix A. In addition, simulation results for the PFC converter are given to demonstrate the operation of the converter system.

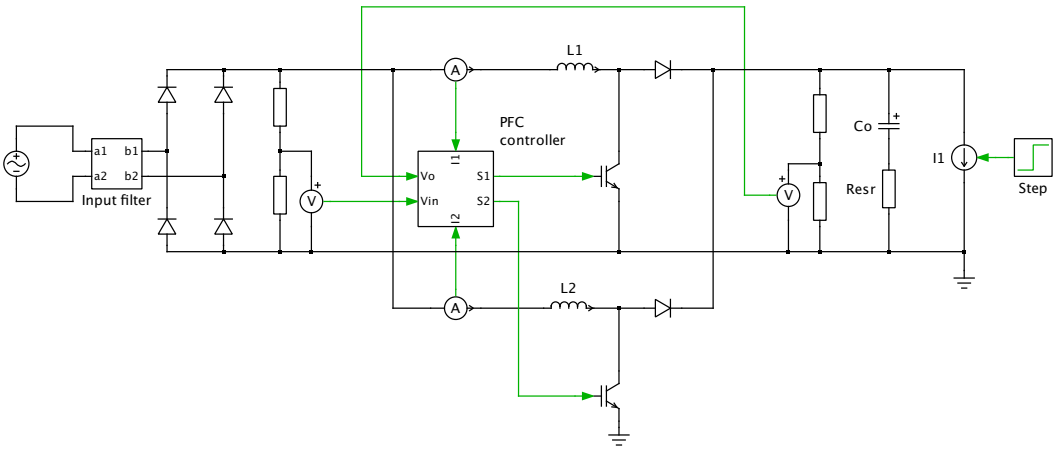


Fig. 1: Schematic diagram of interleaved boost PFC converter.

2 Modeling

2.1 PFC controller features

The PFC controller is largely based on the commercially-available UCC28070 PFC control IC [1]. The key functional features of this controller are listed as follows:

- Current control loop based on average current mode control and interleaved switching.
- Transconductance-based error amplifiers.
- Synthesis of inductor current downslope signal.
- Frequency dithering for EMI distribution.

Table 1: PFC converter parameters.

Input AC voltage	230 V_{rms}, 50 Hz
Output DC voltage	400 V
Rated power	600 W
Switching frequency	50 kHz
Ripple factor, k_{ripple}	50%
L_i	2.17 mH
C_o	600 μF
Input voltage sense gain	3/400
Output voltage sense gain	3/400
Inductor current sense gain	2

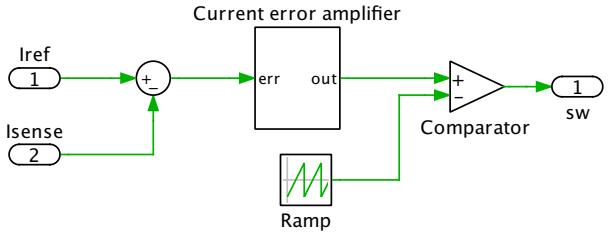


Fig. 2: Switching signal generation with average current mode control.

The modeling of the PFC controller using PLECS is described in the remainder of this section. The protection features such as overvoltage protection and peak current limiting are not modeled since the purpose of the simulation model is to verify the system operation under normal rather than overload conditions.

2.2 Average current mode control

An average current mode control (ACMC) strategy regulates the average boost inductor current to a reference waveform that has the same shape as the rectified mains voltage. The operating principle of ACMC is illustrated in Fig. 2. The output of the current error amplifier is compared directly with a ramp waveform to generate a switching signal. Since the current error amplifier effectively filters the current error signal, average current mode control has an inherent higher immunity to noise than peak current mode control. Further information about average current mode control can be found in [2].

2.3 Inductor current downslope synthesis

In order for ACMC to function correctly, the complete inductor current must be sensed, including the current upslope when the switch is on and the downslope when the switch is off. The inductor current upslope can be measured by placing a current transformer (CT) in series with the switch. Instead of using an additional CT in series with the power diode to measure the current downslope, the downslope is constructed in the UCC28070 using a special synthesis function.

In PLECS, the inductor current sense circuit is modeled in an idealized fashion by directly measuring the inductor current and applying a gain equivalent to the current transformer gain. For a behavioral simulation, the details of the current transformer and downslope synthesis function are unnecessary and a simplified functional representation is sufficient.

2.4 Transconductance amplifier

Transconductance amplifiers are used in the UCC28070 for both the voltage and current error amplifiers. The transconductance amplifier outputs a current signal proportional to the voltage difference at its inputs. In PLECS, a behavioral model of the transconductance amplifier is created with a Gain block and a Current Source (Controlled) block, as shown in Fig. 3.

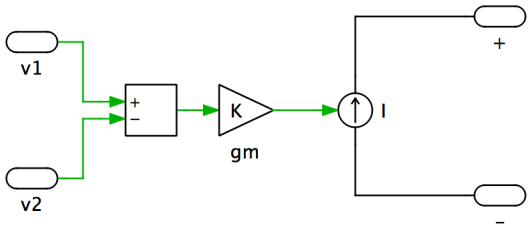


Fig. 3: Implementation of transconductance amplifier. Output current is equal to $g_m(v_1 - v_2)$.

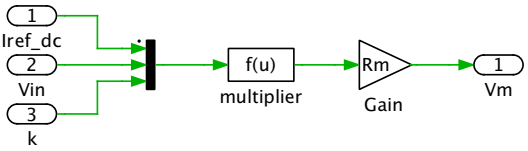


Fig. 4: Modeling the multiplier and termination resistance using a Function and Gain block.

2.5 Multiplier

The multiplier creates a half-sinusoidal reference current for the current loop by multiplying the rectified mains voltage, V_{in}, by the voltage controller output, $I_{ref\,dc}$. The output of the multiplier is a current signal that is converted into a voltage with a termination or gain resistance, R_m. The multiplier output voltage is given as follows:

$$V_m = 17\mu A \cdot \frac{V_{in\,sense}(I_{ref\,dc} - 1)}{k_{vff}} \cdot R_m \tag{1}$$

Inside the PFC controller, k_{vff} is a quantized feedforward variable that is a function of peak input AC voltage. At the operating point of $V_{in} = 325$ V, k_{vff} is 2.922, assuming the gains of the input and output voltage sense circuits are the same [1].

In PLECS, the multiplier is modeled as shown in Fig. 4 with a Function block that implements Eq. (1) and a Gain block that represents the multiplier termination resistance, R_m. The feedforward variable, k_{vff}, is kept constant since it is assumed the input voltage remains constant.

2.6 Interleaved switching and frequency dithering

The PFC controller uses interleaved switching in order to reduce the overall input current ripple. The two switch signal outputs have a phase displacement of $180°$. At a duty cycle of 0.5, the ripple currents in each inductor completely cancel each other and at other duty cycles, partial current ripple cancellation is achieved, reducing the overall current ripple compared to a single-inductor converter. To model the interleaved switch signal outputs with ACMC, the ramp signals used for the switching signal generation are interleaved by $180°$.

The PFC control IC also offers frequency dithering to spread the EMI spectrum and thus simplify the filter requirements. Since the switching frequency is derived from the ramp frequency, frequency dithering is modeled in PLECS by varying the ramp frequency. A simple means of generating a variable frequency ramp signal is to use a resettable integrator configured as shown in Fig. 5. The DC input signal, dc_val, is calculated at the beginning of each switching period such that the integrator output reaches $ramp\_ampl$ at the end of the switching period. The DC input signal is calculated using:

$$dc\_val = ramp\_ampl \cdot f_s \tag{2}$$

where f_s is the reference switching frequency. The variable switching frequency reference is modeled in PLECS using a triangular waveform as shown in Fig. 6. The base frequency, frequency deviation and dither rate are adjusted using the parameters f_{base}, $\triangle f_s$ and t_{dither}.

The resettable integrator is implemented in PLECS using the C-Script block, since it can reset the integrator state based on the output value without creating an algebraic loop. The integrator itself is implemented as a continuous differential equation.

At the beginning of the switching period, the C-Script block measures f_s and calculates dc_val. When the integrator value reaches the peak ramp amplitude, the integrator is reset and the next switching period begins. To generate the interleaved ramp signal, a second C-Script block is used. Instead of calculating dc_val again, it uses the dc_val calculated by the first C-Script block to ensure the volt-seconds product applied to each inductor is consistent.

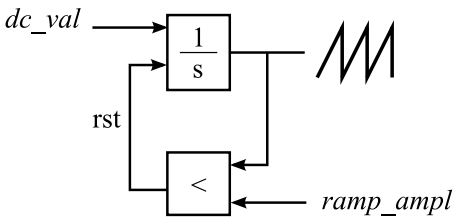


Fig. 5: Generation of variable-frequency ramp signal using a resettable integrator.

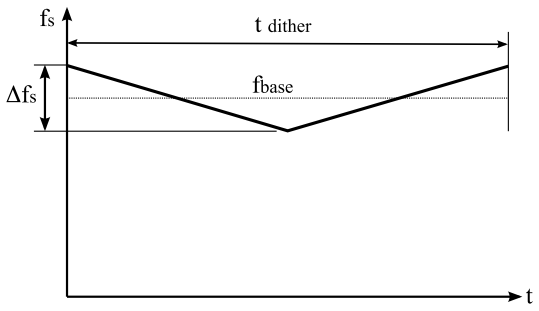


Fig. 6: Frequency dithering parameters.

3 System Dimensioning

3.1 Output capacitor sizing

The output capacitor is sized to limit the voltage fluctuations induced by the inflow of AC power from the input stage to 2% of the nominal DC output voltage. Thus the output DC voltage is maintained in the range of $396 - 404$ V. Using the procedure detailed in Appendix C, the DC capacitance is calculated to be 597 μF.

3.2 Inductor design

The inductors are designed to operate in continuous conduction mode (CCM). In CCM, the inductor current is continuous and does not reach zero, although in a PFC converter operating with a fixed switching frequency, there may be short periods of discontinuous conduction at the mains voltage zero-crossing.

The inductance is calculated to limit the peak current ripple in each inductor to a limit defined by:

$$\triangle I_L = \frac{k_{ripple} \cdot \hat{I}_i}{n} \tag{3}$$

where $\hat{I}_i$ is the peak input current at full load, k_{ripple} is the ripple factor and n is the number of inductors. A current ripple factor of 0.5 is chosen since this has been shown to provide a good compromise between inductor size, inductor core losses and input filter cutoff frequency [3].

The peak input current in Eq. 3 is calculated using:

$$\begin{aligned} \hat{I}_i &= \frac{2P_o}{\hat{V}_i} \\ &= 3.69A \end{aligned} \tag{4}$$

Thus for $k_{ripple} = 0.5$ and $n = 2$, Eq. (3) is solved to give $\triangle I_L = 0.922$ A.

The inductance is now calculated to limit the maximum current ripple to $\triangle I_L$ under the worst-case conditions using the equation derived in Appendix D:

$$L = \frac{V_{dc}}{4 \triangle I_L f_s} \tag{5}$$

Calculating the worst case inductance for $f_s = 50$ kHz and $V_{dc} = 400$ V gives $L = 2.17$ mH.

4 Controller Design

4.1 Current controller

The current controller, based on a type 2 error amplifier, is designed by first obtaining the frequency response of the converter operating in open-loop current control mode. Open-loop current control is achieved

by setting the modulation index for the inner modulation loop to a fixed value that produces the desired output current. The circuit for obtaining the frequency response of the open current loop is shown in Fig. 7.

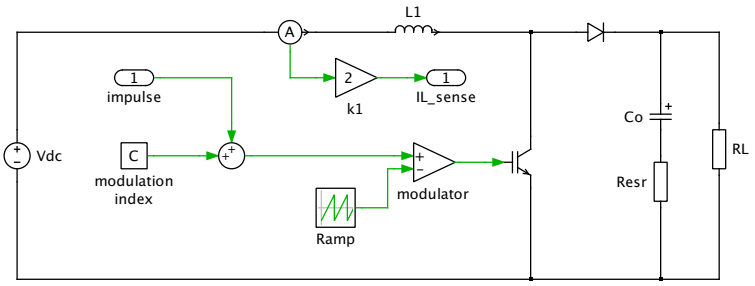
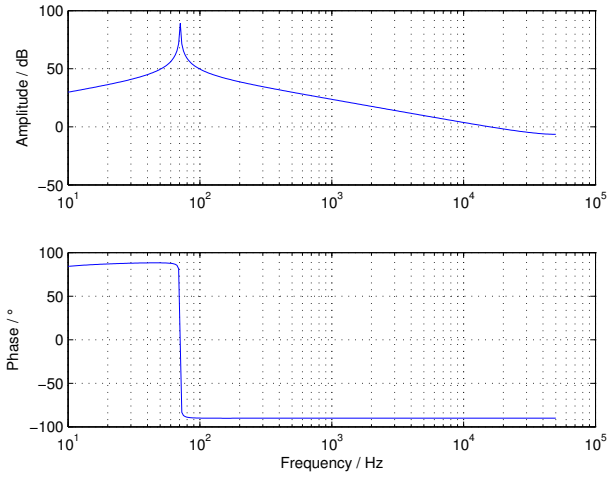


Fig. 7: Circuit for obtaining frequency response in open-loop current control mode. An impulse is added to the modulation index and the response is measured at the sensed current output.

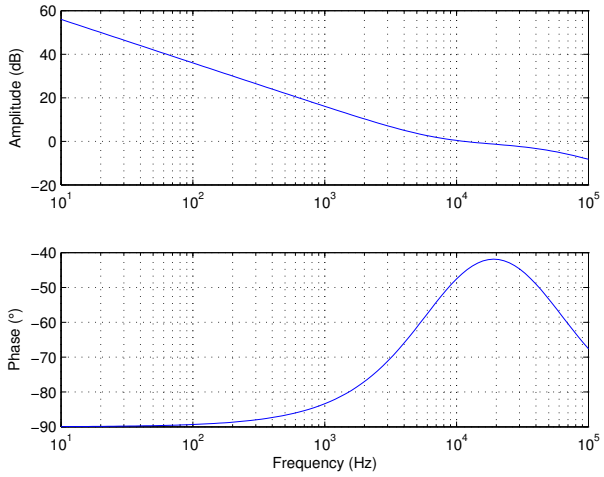
The frequency response is obtained using the PLECS Impulse Response Analysis Tool. An input perturbation is applied by summing an impulse with the modulation index, and the output response is obtained from the sensed current output. The current through a single boost inductor is measured since an individual controller is used for each boost inductor current.

In order to run the analysis, the steady state operating point of the circuit must be set. The load is reduced by a factor of two to $300\ \mathrm{W}$ since a single boost inductor processes only half the output power. The input rectifier is replaced with a DC source set to $200\ \mathrm{V}$, since this is the input voltage at which the maximum current ripple occurs. The modulation index is then adjusted to produce an output voltage of $400\ \mathrm{V}$.

Running the Impulse Response Analysis of the open current loop at this operating point yields the frequency response shown in Fig. 8(a). It can be seen that above the resonant frequency of the capacitor and inductor, the frequency response has an inductive characteristic. The gain has slope of $-20\ \mathrm{dB/decade}$ and the phase shift is $-90°$.



(a) Open-loop system.



(b) Current controller.

Fig. 8: Current loop Bode plots.

To design the current controller, the unity gain bandwidth of the current loop is set to $f_s/3 = 16.67\ \mathrm{kHz}$ in order to provide a fast-acting current response. At this frequency, the open-loop current gain is $-0.6\ \mathrm{dB}$; therefore, the current error amplifier gain is set to $0.6\ \mathrm{dB}$ to achieve a unity loop gain. At the unity gain frequency, the phase margin is set to $45°$, a good balance between rise and settling time.

To achieve this phase margin, the type 2 compensator is centered at $f_s/3$ and its phase shift is precisely set to $-45°$ using the k-factor design approach described in Appendix E. The k-factor required to achieve this boost value is 2.414, yielding a location for the zero and pole of $6.91\ \mathrm{kHz}$ and $40.2\ \mathrm{kHz}$, respectively.

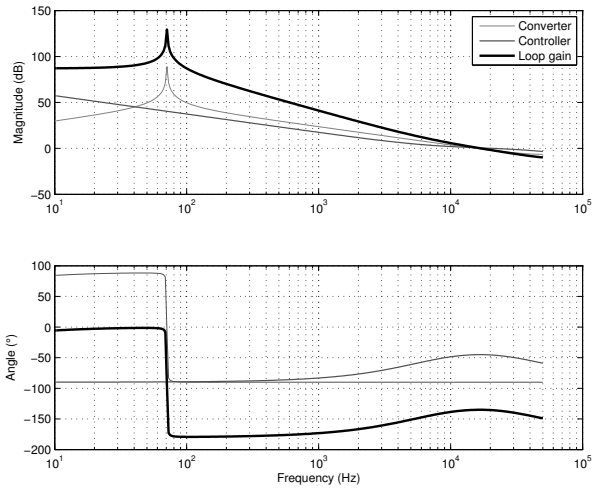


Fig. 9: Loop gain of current-controlled system for predicting closed-loop response.

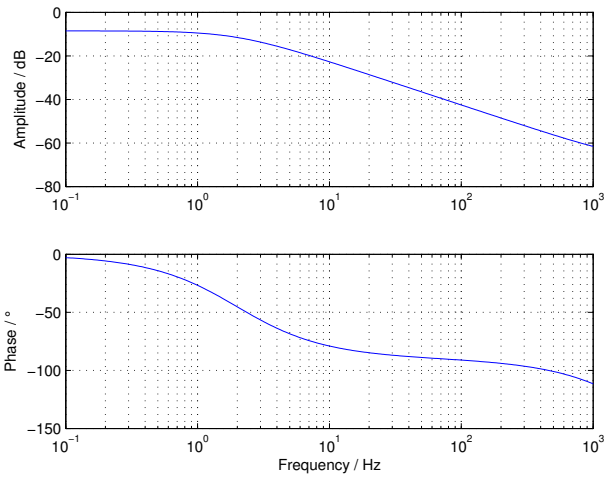


Fig. 10: Frequency response of converter with open-loop voltage control.

Calculating the component values for the type 2 compensator yields $R_1 = 10.1\ \text{k}\Omega$, $C_1 = 2.15\ \text{nF}$, $C_2 = 0.369\ \text{nF}$. The equations for a type 2 transconductance-based error amplifier are given in Appendix F. A Bode plot of the current controller is displayed in Fig. 8(b).

To predict the closed-loop response of the current control loop, the magnitude and phase responses of the open-loop converter and controller are added to obtain the loop gain. The loop gain of the current loop is depicted in Fig. 9.

4.2 Voltage controller

In order to design the voltage controller, the small-signal frequency response of the converter operating in open-loop voltage control mode is required. The converter is operated in open-loop voltage control mode by setting the reference current, the control variable, to a fixed value that sets the output voltage to $400\ \text{V}$. Using the Impulse Response Analysis Tool, the frequency response of the converter is obtained by perturbing the reference current signal and observing the response at the output voltage sense circuit.

The Impulse Response Analysis is performed at the operating point of $P_o = 600\ \text{W}$, $V_{in} = 200\ \text{V}$, $V_o = 400\ \text{V}$. For simplicity, the inner current loop is formed from a single boost phase leg. The gain of the current sensor is halved in order to double the output current of the single boost phase leg and thus produce the correct total current for a given reference current. The boost inductance is doubled to reduce the current ripple.

The frequency response of the open voltage loop is depicted in Fig. 10. It can be seen that the system has a first-order pole at $2\ \text{Hz}$. Below the unity gain frequency of the current loop, the current loop behaves as an ideal current source, allowing the converter to be approximated with an RC circuit.

A type 2 error amplifier is also used for the voltage controller. The design requirements for the voltage controller are to provide as high a unity gain frequency as possible in order to ensure a fast response to step changes in the load. The phase margin at the crossover frequency must be at least $45°$ and the attenuation at $100\ \text{Hz}$ must be below $-34\ \text{dB}$ to limit the amplification of the output voltage ripple to 2%, an arbitrary value. If the $100\ \text{Hz}$ output voltage ripple is coupled into the voltage control loop, the current reference signal becomes distorted, creating a third harmonic current in the input current.

The k-factor design approach is not used for the voltage controller design since the phase shift is not the only design constraint. In addition to the phase margin constraint, the closed-loop system must meet the $100\ \text{Hz}$ attenuation constraint and have as high a bandwidth and DC gain as possible.

The controller design is optimized by iterating the pole and zero locations based on the predicted loop gain. The design objectives are achieved with the following controller parameters: $A_v = 18\ \text{dB}$, $f_z = 3\ \text{Hz}$, and $f_p = 20\ \text{Hz}$. The Bode plot of the type 2 controller and the resultant loop gain are shown in Fig. 11. Measuring the key performance characteristics from the loop gain plot indicates the unity gain frequency of the voltage control loop is $60\ \text{Hz}$, the phase margin is $65°$ and the attenuation at $100\ \text{Hz}$ is $-38\ \text{dB}$.

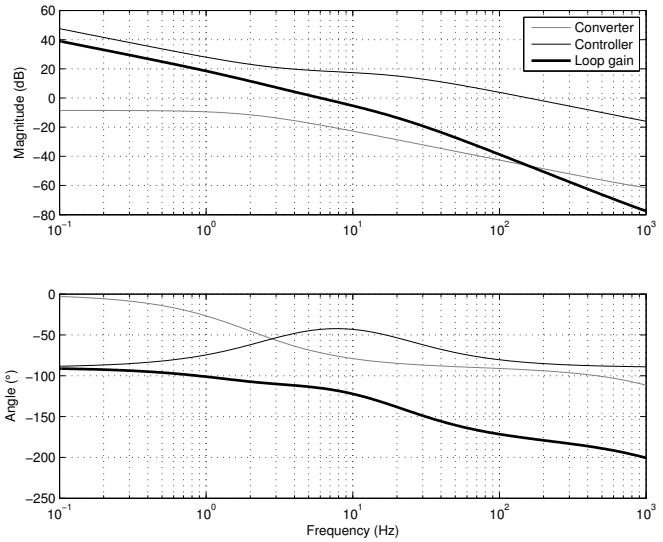


Fig. 11: Frequency response of voltage loop.

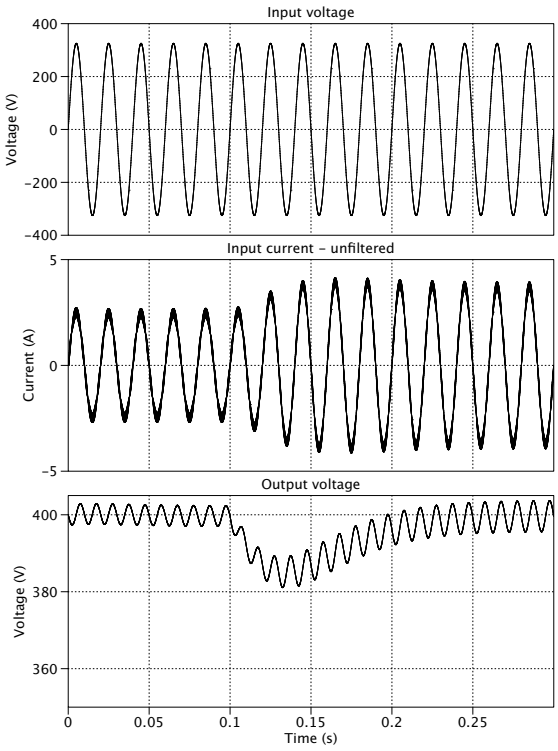


Fig. 12: Converter response to a step change in load current of 1.0 to 1.5 A at $t = 1.5$ s.

Using the procedure outlined in Appendix F, the component values for the transconductance amplifier are calculated to be $R_1 = 17.6$ kΩ, $C_1 = 668$ nF, $C_2 = 118$ nF.

4.3 Multiplier gain

The multiplier gain, set with the resistor R_m, is calculated to limit the multiplier output voltage at full load to $V_m = 3.7$ V. This sets the average peak measured inductor current to 1.85 A and the total average peak input current to 3.7 A. Rearranging Eq. (1) to solve for R_m yields:

$$R_m = \frac{k_{vff} V_m}{17\mu A \cdot V_{in\,sense}(I_{ref} - 1)} \tag{6}$$

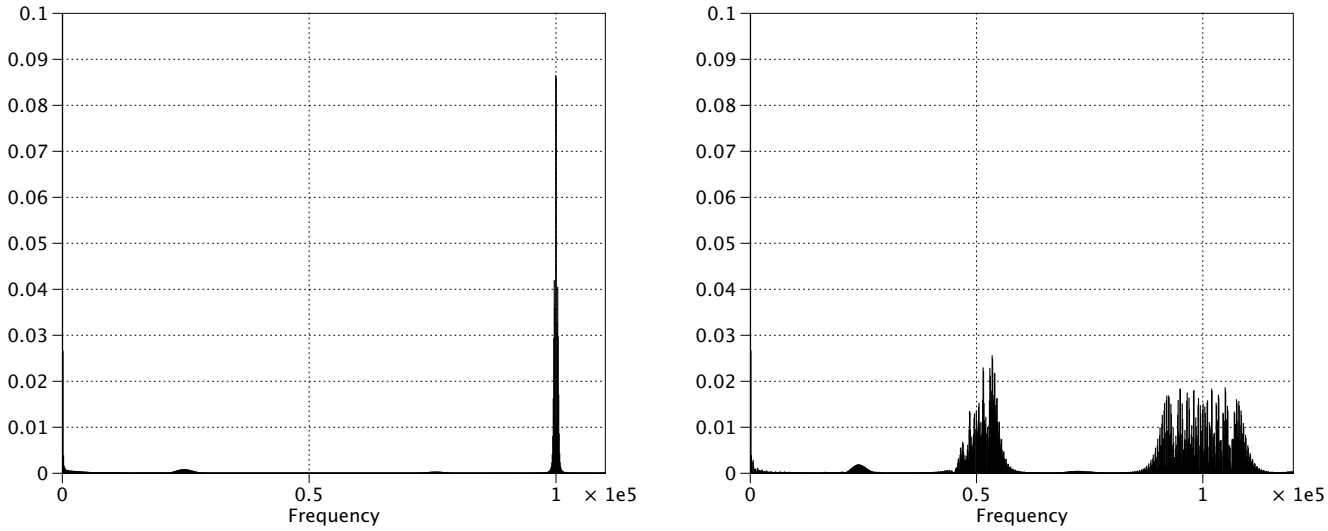
Solving at the peak output power where $V_{in\,sense} = 325 \cdot \frac{3}{400}$ and $I_{ref\,dc} = 4$ yields $R_m = 87.0$ kΩ.

5 Simulation Results

Simulation results of the PFC converter system supplying a constant-current load are presented in Fig. 12. At $t = 0.1$ s. the load current is increased from 1.0 to 1.5 A, causing the output voltage to decrease. The voltage controller compensates for the error by increasing the reference current, and the system settles within 0.15 s.

The frequency spectrum of the unfiltered input current is shown in Fig. 13. With a constant switching frequency of 50 kHz, harmonic currents appear at 100 kHz due to the interleaved switching. As shown in Fig. 13(a), the peak amplitude of the 100 kHz harmonic current is 86 mA.

The effect of frequency dithering can be seen in Fig. 13(b). The switching frequency is varied by ± 5 kHz from the base frequency of 50 kHz at a rate of 500 Hz. It can be seen that the peak amplitude of the current harmonics in the vicinity of 100 kHz is reduced significantly to 18 mA due to the smearing effect of the dither.



(a) Switching frequency 50 kHz.

(b) Switching frequency = 50 ± 5 kHz. Dither rate = 500 Hz.

Fig. 13: Frequency spectrum of unfiltered input current. Values are in Amperes.

6 Conclusion

PLECS is a useful program for modeling connected electrical and control systems. In this application note, a PFC boost converter was modeled and designed using the PLECS Analysis Tools. The PFC converter model included interleaved switching to reduce the input current ripple and frequency dithering to spread the high-frequency current harmonics. The design of the current and voltage controllers for the PFC converter was assisted by the PLECS Impulse Response Analysis Tool. Using this tool, the open-loop transfer functions of the current and voltage loops were obtained and the controllers were designed to meet design criteria such as the phase margin constraint. The PLECS AC Sweep Tool was used to obtain the transfer function of the controller and calculate the loop gains, allowing the closed-loop performance of the system to be predicted. Simulation results demonstrate the operation of the converter, and the attached model files can be used and adapted to other similar PFC converter designs.

Appendices

A Simulation Files - PLECS Blockset

Example files used for the generation of the Bode plots and simulating the complete PFC system using PLECS Blockset accompany this application note:

- *Iloop_impulse.mdl*: For obtaining the frequency response of the converter in open-loop current control mode.
- *Vloop_impulse.mdl*: For obtaining the frequency response of the converter in open-loop voltage control mode.
- *Type2_Icontroller.mdl*: For obtaining the frequency response of the current controller.
- *Type2_Vcontroller.mdl*: For obtaining the frequency response of the voltage controller.
- *type2_controller_bode.m*: For generating the Bode plot of the current or voltage controller.
- *bode_add_blockset.m*: A helper function for estimating the loop gain by adding the Bode plots for the converter and controller.
- *plbode.m*: A helper function for generating Bode plots that can be modified by the user for a specific model.
- *PFC_f_50.mdl*: Complete simulation model with a constant switching frequency of 50 kHz.
- *PFC_f_dither.mdl*: Complete simulation model with a switching frequency of 50 kHz $\pm$ 50kHz.

To generate the Bode plot of the converter in open-loop current control mode, open the file *Iloop_impulse.mdl* and run the Impulse Response Analysis Tool. The result, computed at 101 points over the frequency range 10 Hz $-$ 100 kHz, is stored in a struct named `Iconverter`. The same process can be used for the converter in open-loop voltage control mode.

To generate the Bode plot of the type 2 current controller, run the function, `Icontroller=type2_controller_bode('Type2_Icontroller', [10 100e3], 101)`. The same process can be used to obtain the frequency response of the voltage controller.

The loop gain Bode plot is obtained by adding the generated frequency responses with the function call `bode_add_blockset(Iconverter, Icontroller)`.

B Simulation Files - PLECS Standalone

Example files used for the generation of the Bode plots and simulating the complete PFC system using PLECS Standalone accompany this application note:

- *Iloop_impulse.plecs*: For obtaining the frequency response of the converter in open-loop current control mode.
- *Vloop_impulse.plecs*: For obtaining the frequency response of the converter in open-loop voltage control mode.
- *Type2_Icontroller.plecs*: For obtaining the frequency response of the current controller.
- *Type2_Vcontroller.plecs*: For obtaining the frequency response of the voltage controller.
- *bode_add.m*: A helper function for estimating the loop gain using MATLAB by adding the Bode plots for the converter and controller.
- *bode_add.py*: A helper function for estimating the loop gain using Python by adding the Bode plots for the converter and controller.
- *PFC_f_50.plecs*: Complete simulation model with a constant switching frequency of 50 kHz.

- *PFC_f_dither.plecs*: Complete simulation model with a switching frequency of $50\ \text{kHz} \pm 50\text{kHz}$.

To generate the Bode plot of the converter in open-loop current control mode, open the file *Iloop_impulse.plecs* and run the Impulse Response Analysis Tool that is configured under *Simulation > Analysis Tools*. The result is computed at 101 points over the frequency range $10\ \text{Hz} - 100\ \text{kHz}$. Save the resultant Bode plot as a *csv* file. To obtain the Bode plot for the type 2 current controller, open the file *Type2_Icontroller.plecs* and run the AC Sweep Tool. Save the Bode plot of the controller as a separate *csv* file.

To calculate the loop gain of the current control loop, add the saved frequency responses for the converter and controller and plot the result using MATLAB or Python. The files *bode_add.m* and *bode_add.py* can be used to calculate the loop gain.

The files *Vloop_impulse.plecs* and *Type2_Vcontroller.plecs* also have predefined Impulse Response and AC Sweep analyses and allow the loop gain of the voltage control loop to be calculated in the same way as for the current control loop.

C Calculating the Output Filter Capacitance

The power flowing from the input stage into the DC capacitor is single-phase AC power because both the input voltage and current are sinusoidal. The AC power has a large ripple component, oscillating between 0 and 2π at a frequency of $100\ \text{Hz}$ as shown in Fig 10. The equation for the AC power is given by:

$$P_{ac}(t) = P_{dc}(1 - \cos(2\omega t)) \tag{7}$$

The output capacitor is sized to limit the output voltage ripple caused by the fluctuating AC input power. Integrating Eq. (7) to find the energy yields:

$$E(t) = \frac{P_{dc}}{2\omega}\sin(2\omega t) \tag{8}$$

The peak fluctuation in energy can be found by evaluating Eq.(8) at $2\omega t = \pm\frac{\pi}{2}$, giving:

$$\triangle E = \frac{P_{dc}}{\omega} \tag{9}$$

The capacitor size can be determined by equating Eq. (9) with the capacitor energy equation, $\triangle E = 0.5C\triangle V^2$. The capacitance can now be expressed as a function of the voltage deviation limits:

$$C = \frac{2P_{dc}}{\omega(V_{max}^2 - V_{min}^2)} \tag{10}$$

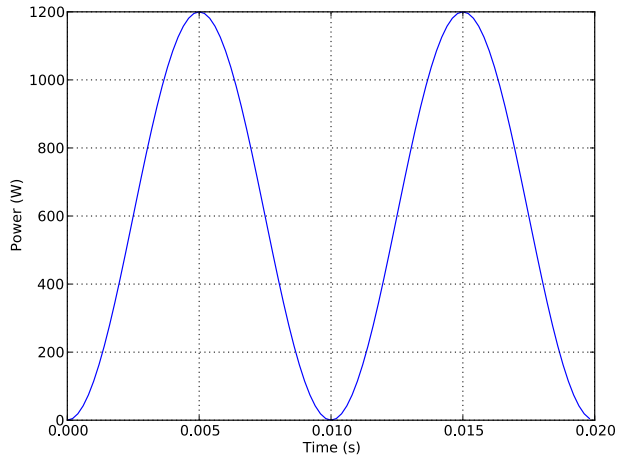


Fig. 14: AC power flowing through the PFC input stage.

D Design of the Boost Inductor

The boost inductor is sized in order to limit the peak ripple current to a specified value, $\triangle I_L = k_{ripple}\hat{I}_i$. In continuous conduction mode (CCM), the inductance can be calculated by applying the equation $\triangle v = L\frac{\triangle I_L}{\triangle t}$ during the turn-off period. This yields the following equation for the inductance:

$$L = \frac{(V_{dc} - \hat{V}_i)d'}{\triangle I_L f_s} \tag{11}$$

where

- d' is the off time ratio, equivalent to $1 - d$.
- f_s is the switching frequency.
- $\hat{V}_i$ is the peak input voltage.

By plotting a normalized graph of L vs d, where

$$d = 1 - \frac{\hat{V}_i}{V_{dc}} \tag{12}$$

it can be seen that the worst-case inductance value is obtained when $d = 0.5$. The equation for the worst-case inductance is obtained from Eq. (11) by substituting in Eq. (12) and the worst case d, giving:

$$L = \frac{V_{dc}}{4\triangle I_L f_s} \tag{13}$$

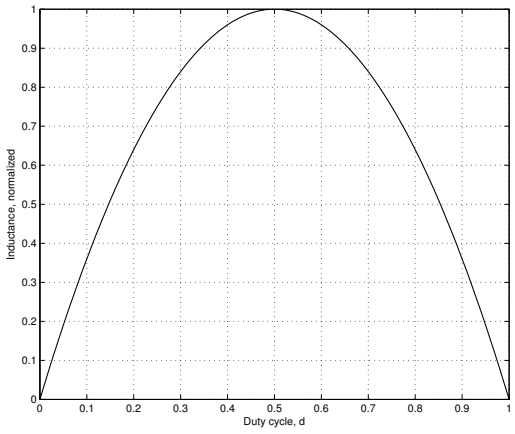


Fig. 15: Normalized boost inductance vs. duty cycle in CCM.

E Designing a Type 2 Amplifier using the K-Factor

The k-factor approach to selecting the location of the zero and pole allows the midband phase boost to be precisely determined rather than by iterating to obtain an appropriate phase boost [4]. The phase boost at the midband frequency, f_1, is calculated by:

$$boost = 2\tan^{-1}(k) - 90^\circ \tag{14}$$

The phase boost is graphically depicted as a function of k in Fig. 16.

The pole and zero locations are then calculated as follows:

$$f_z = \frac{f_1}{k} \tag{15}$$

$$f_p = k \cdot f_1 \tag{16}$$

The effect of different k values on the magnitude and phase plots of the type 2 amplifier can be seen in Fig. 17.

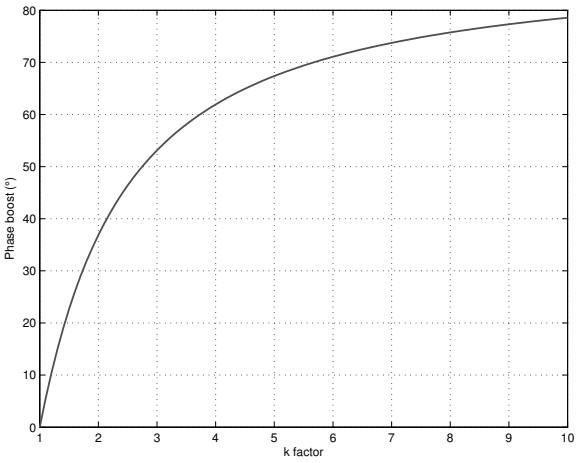


Fig. 16: Phase boost vs. k-factor for type 2 amplifier.

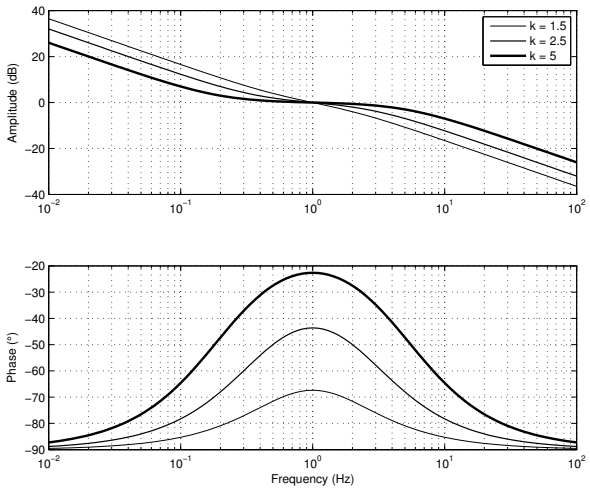


Fig. 17: Effect of k-factor on type 2 amplifier gain and phase.

F Type 2 Transconductance Amplifier Equations

The Bode plot of a type 2 controller is given in Fig. 18 and its implementation using a transconductance amplifier is shown in Fig. 19.

By inspection of the circuit, the midband gain is determined by the resistance. Therefore the resistance is calculated with:

$$R_1 = \frac{k}{g_m} \tag{17}$$

where k, the midband gain, is calculated from the gain A_v (dB) using $k = 10^{\frac{A_v}{20}}$.

In order the calculate the capacitance values that set the zero and pole locations, the transfer function is needed. This transfer function is given by:

$$\frac{v_o}{v_{err}} = g_m \frac{sR_1C_1 + 1}{s^2R_1C_1C_2 + s(C_1 + C_2)} \tag{18}$$

By equating the numerator and denominator to zero, ω_z and ω_p are found:

$$\omega_z = \frac{1}{R_1C_1} \tag{19}$$

$$\omega_p = \frac{C_1 + C_2}{R_1C_1C_2} \tag{20}$$

Since R_1, ω_z and ω_p are known, C_1 and C_2 are calculated as follows:

$$C_1 = \frac{1}{R_1 2\pi f_z} \tag{21}$$

$$C_2 = \frac{1}{2\pi f_p R_1 - \frac{1}{C_1}} \tag{22}$$

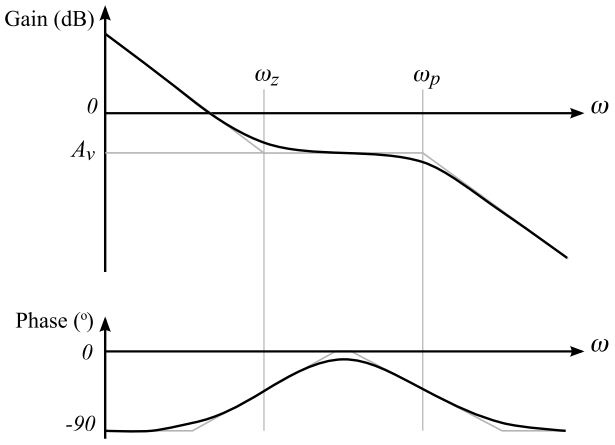


Fig. 18: Bode plot of type 2 controller.

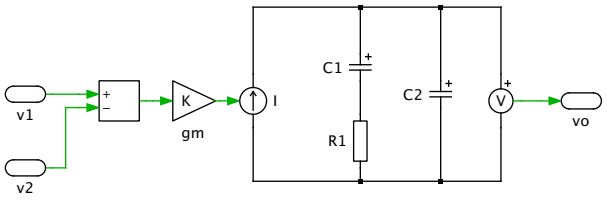


Fig. 19: Type 2 controller using a transconductance amplifier.

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