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THE SIMULATION SOFTWARE PREFERRED
BY POWER ELECTRONICS ENGINEERS

PLECS RT BOX®

Hardware-in-the-Loop (HIL) Platform

Plexim's product line now includes real-time simulation hardware to provide a complete, one-stop solution for modern power electronic system development teams.

Technical Specifications

Processor

Xilinx Zynq Z-7030	
CPU clock speed	1 GHz

Analog input

Channels	16
Resolution	16 bit
Voltage range	-10 ... 10 V
Input type	Differential
Sample rate	2 Msps
Input impedance	1 MΩ, 24 pF
Protection	Overvolt., ESD
Connector	D-SUB 37 pin male

Analog output

Channels	16
Resolution	16 bit
Voltage ranges	-10 ... 10 V 0 ... 10 V -5 ... 5 V 0 ... 5 V
Sample rate	2 Msps
Output impedance	0 MΩ
Output current	⩽ 5 mA
Protection	Short-circuit, Overvolt., ESD
Connector	D-SUB 37 pin female

Digital input

Channels	32
Logic levels	3.3 V (5 V tolerant)
Protection	Overvolt., ESD
Connector	D-SUB 37 pin male

Digital output

Channels	32
Logic levels	5 V, 3.3 V
Output impedance	250 Ω
Protection	Short-circuit, Overvolt., ESD
Connector	D-SUB 37 pin female

Connectivity

Ethernet	RJ-45, Gigabit
High speed interconnect	4 x SFP+, 6.25 Gbps per lane
USB device	USB 2.0 high speed, Type A
Host PC	USB 2.0, Type B
Firmware	SD card

Power supply

Internal	100 ... 240 Vac 50 ... 60 Hz

Size

D x W x H	31 x 25 x 10cm

The PLECS RT Box is a state-of-the-art real-time simulator designed for HIL testing of complex power converter systems. The unit may also be scaled up for more demanding HIL applications, such as modular multi-level HVDC converters.

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Trial license

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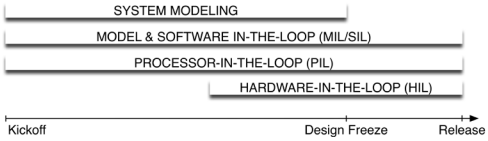
Agile System Design Using PLECS

System modeling is crucial to power electronics product development. It facilitates early design decisions and formulation of system and subsystem requirements. An agile development process based on multiple short design iterations provides opportunities to learn lessons and adjust these requirements.

A system model maintained throughout the development process also serves as a virtual test bed for subsystem iterations. Developing systems using the PLECS toolchain can keep the different subsystems in sync during their respective design iterations.



Using PLECS tools with an agile design flow

"In-the Loop" testing of control software (SIL/PIL) can be applied very early in development, minimizing risk of subsystem incompatibility. As control hardware becomes available, HIL testing can be used to increase test coverage.

The PLECS RT Box, together with the PLECS circuit simulator and PLECS Coder, provides a complete and consistent solution for system-level verification and validation of control software and hardware subsystems.

Code Generation

The PLECS Coder can generate C code from a PLECS model for execution on real-time hardware. This requires the model to be discretized to run at a fixed sample frequency. Due to the fast time constants inherent in power conversion systems, the step size typically is on the order of µs. The ideal step size is a compromise between system model fidelity and accuracy of the simulation results.

To assist the developer with this tradeoff, the PLECS Coder supports simulating generated discretized code within PLECS before it is deployed onto the real-time hardware.

This allows inspecting signal waveforms for different use cases and ensuring they are accurate enough for system testing purposes.

Specialized Switch Models

Specifically for real-time code generation, PLECS' component library includes Power Modules. These blocks implement power-stage topologies such as choppers, 2 and 3-level half bridges, and cascaded half and full bridges, all optimized for real-time simulation of models containing many switches.

Simulation Speed

The most meaningful metric when comparing the "speed" of real-time simulators is overall roundtrip latency, i.e. total time elapsed from measuring inputs to updating outputs. Delays depend on the underlying hardware topology. Several approaches exist, all with tradeoffs.

	DSP	FPGA	SOC
Performance	++	++	+
Flexibility	++	-	++
Latency	--	++	+

HIL hardware implementation options

The PLECS RT Box is based on an SOC, optimizing I/O latency, numerical performance and modeling flexibility. The latest generation of 16-bit ADC and DAC chips ensures excellent signal resolution. The digital capture module can resolve PWM signals at 10 ns.

Outlook

The PLECS RT Box is designed with the future in mind. With its high-speed communication interface, multiple RT Boxes can operate in parallel or in a master/slave arrangement. Such configurations leverage PLECS solver and coder technologies currently being developed, making the platform even more powerful and suitable for complex, large scale real-time simulations.

Plexim's product portfolio now covers all aspects of virtual system testing. We offer a one-stop solution with a unified user experience and the trusted power of PLECS.

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