



PLECS

*DEMO MODEL*

## Single-Phase Battery Charger

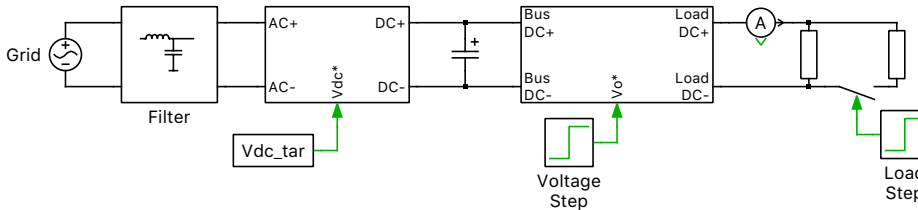
Last updated in PLECS 4.7.1

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# 1 Overview

This demonstration shows a grid-connected battery charger with cascaded AC/DC and DC/DC converters. The AC/DC converter is regulated by a digital PI controller to achieve power factor correction (PFC) and maintain the DC bus voltage at 300 VDC. The DC/DC converter is designed to provide a maximum 120 VDC output at a power rating of 1.4 kW.



**Figure 1: Top-level schematic of the model.**

**Note** This model contains model initialization commands that are accessible from:  
**PLECS Standalone:** The menu **Simulation + Simulation Parameters... + Initializations**  
**PLECS Blockset:** Right click in the **Simulink model window + Model Properties + Callbacks + InitFcn\***

## 2 Model

### 2.1 AC/DC Converter

The AC/DC converter is connected on the AC side via a single stage low pass filter. The topology is an interleaved PFC boost converter, as described in Microchip's application note (AN1278) [1].

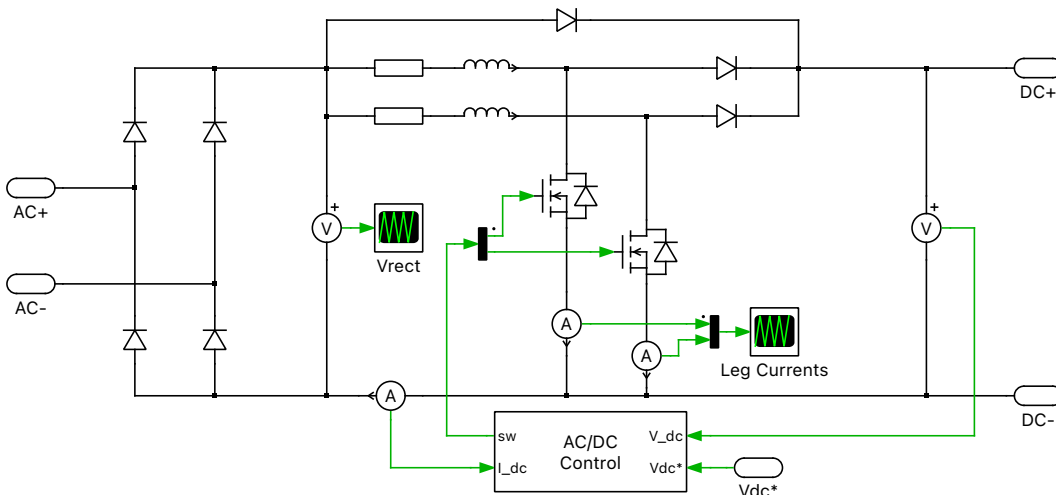
Digital control loops for voltage and current regulation are implemented to achieve power factor correction and regulate the DC side voltage to a desired level. The DC side voltage is sampled and compared to the target bus voltage setpoint. The digital voltage compensator with anti-windup sets a DC current setpoint. This DC setpoint is converted into an AC current setpoint to achieve PFC. The current compensator determines a voltage setpoint, which is converted to a duty cycle. The duty cycle is then used by two symmetrical interleaved PWM blocks.

### 2.2 DC/DC Converter

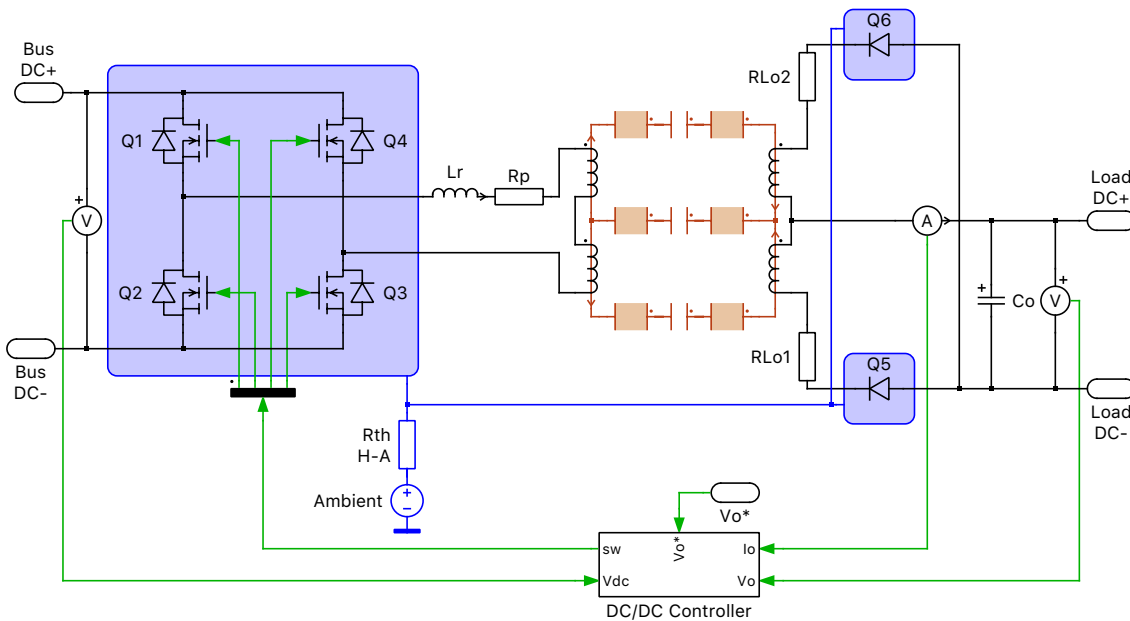
The DC/DC converter implementation is based on a phase-shifted resonant converter, as described in the PLECS demo model "Phase Shift DC-DC Converter with Integrated Magnetics"[2].

### 2.3 Thermal Model

A thermal description is assigned to all four of the MOSFET switches in the full bridge as well as the output diodes. These descriptions can be viewed and edited by double-clicking on the component and selecting **Edit...** from the drop-down menu of the **Thermal description** parameter. The thermal parameters were obtained from datasheets, specifically for the On Semiconductor's SupreMOS superjunction MOSFET and Infineon's IDW75E60 Si power diode. For the two different device types, the thermal impedance chain representing the thermal transitions from the junction to the case are entered directly in the thermal descriptions.



**Figure 2: Schematic of the AC/DC converter.**



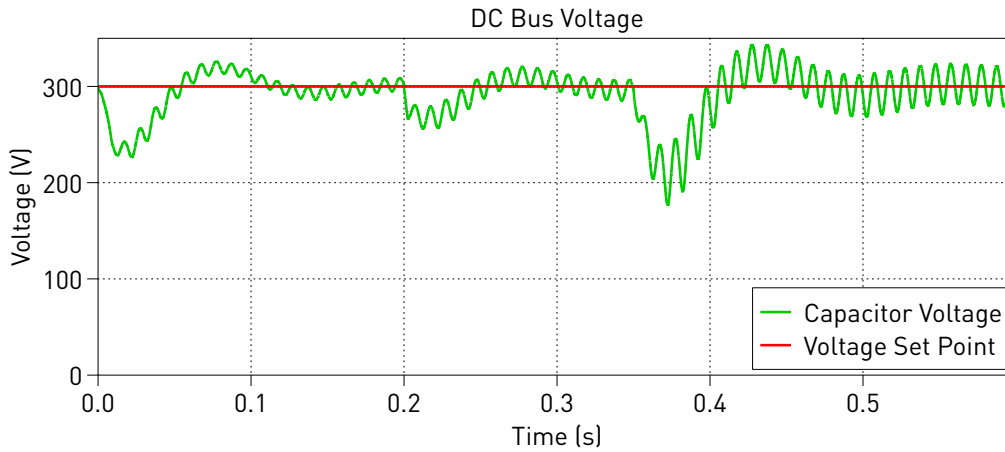
**Figure 3: Schematic of the DC/DC converter.**

Also note that the MOSFET model was customized to permit modeling multiple devices connected in series and parallel. The number of parallel or series connections can be configured in the parameter window of the MOSFETs. An equal distribution of current and voltage in both parallel- or series-connected MOSFETs is assumed. The thermal parameters are automatically scaled to reflect the number of devices and their configuration.

Since the three heat sink components are connected together, all six devices dissipate heat into the same heat sink. A thermal resistance connects the heat sink with the temperature of the ambient air. The thermal descriptions for the MOSFETs and diodes are stored in a private thermal library in the directory /single\_phase\_battery\_charger\_plects.

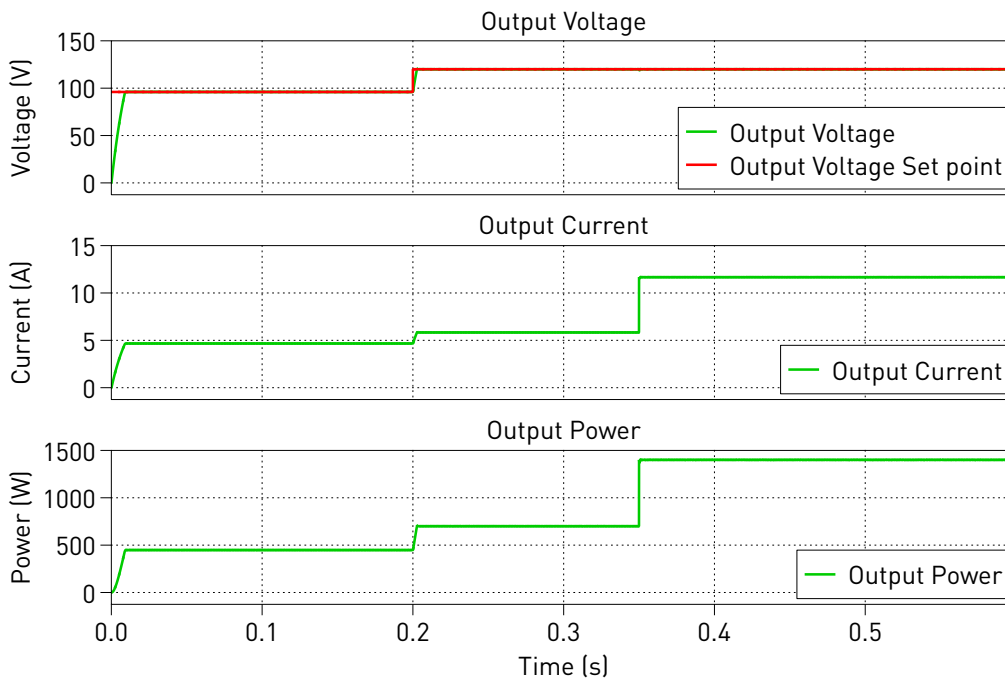
### 3 Simulation

Run the simulation with the model as provided to view the grid side, bus capacitor, and load voltage waveforms. The AC/DC converter is regulated to maintain the bus voltage at 300 VDC.

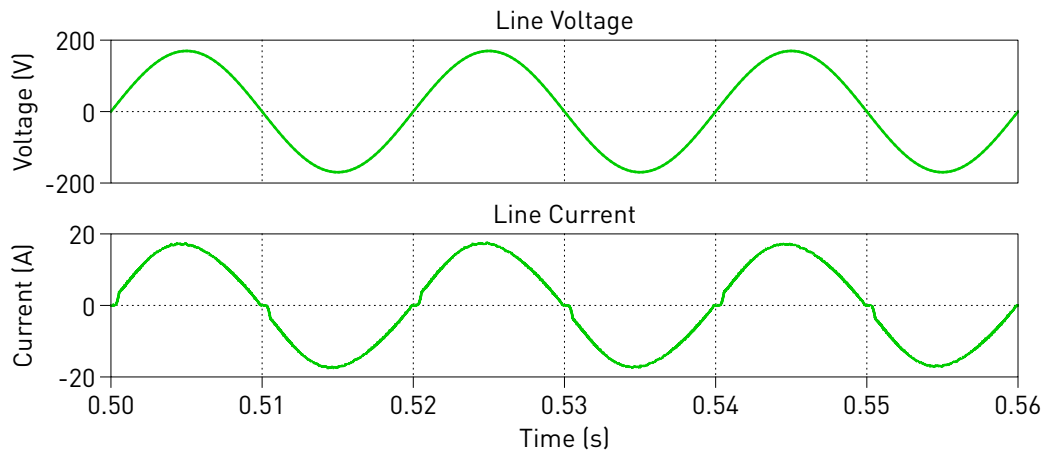


**Figure 4: Simulated DC link voltage.**

Initially the output voltage is regulated to 96 VDC, and at  $t = 0.2$  s, the output reference voltage is stepped to 120 VDC. This voltage step change causes the bus capacitor to sag as it is discharged to provide increased load current. The voltage is regulated back to the 300 VDC setpoint by the AC/DC converter. The bus capacitor voltage can be seen in the “DC Bus” plot, shown above. At  $t = 0.35$  s, the output reference voltage is maintained at 120 VDC and the load is doubled. The bus capacitor is again discharged by the increase in load current. The output current and voltage can be seen in the “Output” plot Fig. 5. The AC/DC and DC/DC converter result in PFC, as can be seen in the “AC Input” plot Fig. 6.



**Figure 5: Simulated output characteristics.**



**Figure 6: Simulated grid characteristics.**

## 4 Conclusion

This demo model shows a grid-connected battery charger with cascaded AC/DC and DC/DC converters. The system is controlled in each stage with cascaded control loops for current and voltage. The DC/DC converter is realized with a phase-shifted resonant converter and its thermal behavior is analyzed using the PLECS thermal domain. The magnetic characteristic of the two parallel E70/33/32 cores is implemented with magnetic components from the PLECS component library such as Air Gaps and Linear Permeances. This way different system level optimization goals such as weight (considering magnetics), losses (considering thermal aspects) and stability can be analyzed and traded off against each other.

## References

- [1] V. Skanda and A. Nahar, *Interleaved Power Factor Correction (IPFC) Using the dsPIC DSC*, DS01278A, Microchip Technology, 2009.
- [2] U. Badstuebner and J. Biela and B. Faessler and D. Hoesli and J.W. Kolar, *An Optimized 5 kW, 147 W/in<sup>3</sup> Telecom Phase-Shift DC-DC Converter with Magnetically Integrated Current Doubler*, Applied Power Electronics Conference and Exposition (APEC), 2009, Twenty-Seventh Annual IEEE, pp. 21-27, 15-19 Feb. 2009.

## Revision History:

PLECS 4.3.1	First release
PLECS 4.6.7	Improve controller performance
PLECS 4.7.1	Using the new Variable Phase PWM library block

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