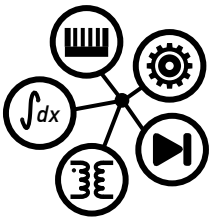

PLECS

DEMO MODEL

LLC Variable Frequency Resonant Converter

Last updated in PLECS 4.3.1

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1 Overview

This demonstration shows an isolated DC/DC resonant converter operated under frequency control. The output voltage of the converter is controlled by changing the switching frequency of the semiconductors. Zero-Voltage Switching (ZVS) is used to reduce switching losses, allowing the operation of the converter at higher switching frequencies.

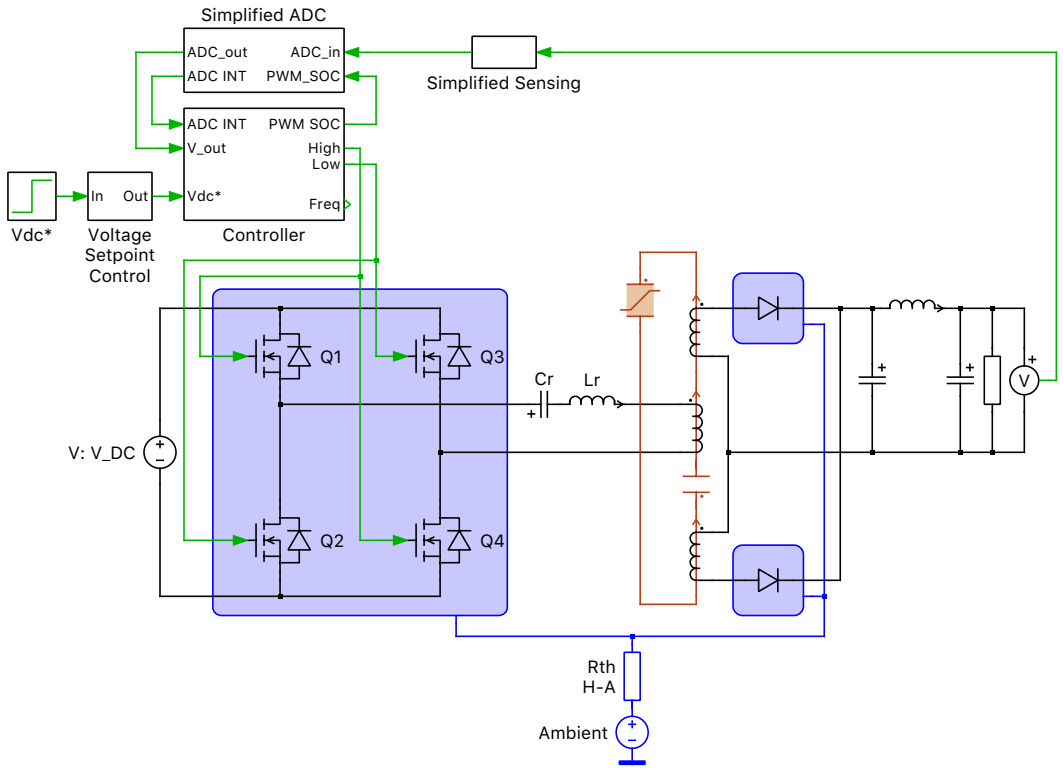

Figure 1: LLC variable frequency resonant converter

Note This model contains model initialization commands that are accessible from:

PLECS Standalone: The menu **Simulation + Simulation Parameters... + Initializations**

PLECS Blockset: Right click in the **Simulink model window + Model Properties + Callbacks + InitFcn***

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2 Model

2.1 Power Circuit

The LLC converter is a DC/DC converter with a front end H-bridge. The AC side of the H-bridge is connected to the primary side of a high frequency transformer via a series-connected resonant inductor and capacitor. The magnetizing inductance of the transformer, along with the inductor and capacitor, form the LLC resonant tank. The secondary side of the transformer is connected to a full wave diode rectifier to convert the AC transformer output to a high ripple DC voltage that is then filtered to provide a low ripple DC voltage output.

The LLC converter is often operated under zero-voltage switching (ZVS) operation where each FET (e.g., Q1) is turned on when the current is still flowing in its respective anti-parallel diode (e.g., D1). Therefore, only the forward voltage drop of the diode is applied to the FET, which is small compared to the DC input voltage. This results in negligible turn-on loss in the device and contributes to the reduction of overall losses. During ZVS operation, the FETs are turned off in a region where they conduct current. This results in hard-switching of the devices, generating turn-off switching losses, as shown below.

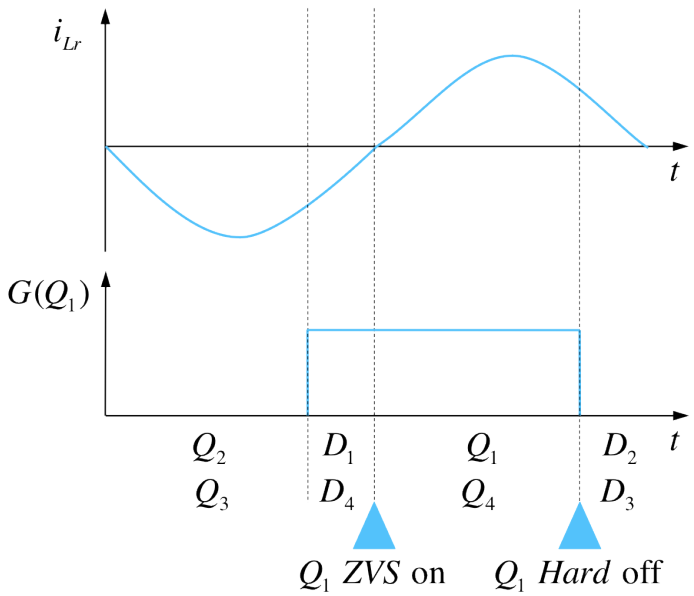

Figure 2: ZVS switching and hard switching

During turn-off and turn-on events, the body capacitor of each FET is charged and discharged, respectively. For circuits where the FETs (not the reverse diodes) experience hard-switching during turn-on, the charge stored in the body capacitor is dissipated through the FET, adding to the switching losses. These losses can be captured in simulation (without adding a capacitor parallel to the FET) by simply including them in the thermal loss look-up tables for a specific part. When measuring the switching energy losses of FETs for certain operation points to generate the loss look-up table, it is important to include the charge stored in the FET body capacitor in the loss measurements. A major advantage of ZVS for FETs, in addition to eliminating turn-on losses, is that the energy stored in the body capacitance is recycled into the circuit [1], assuming there is enough blanking time between turn-off of Q1/Q4 and turn-on of Q2/Q3. Therefore, in soft-switching topologies operated with ZVS, turn-off losses can be overestimated by 10 to 20% [2], if the effects of the capacitive elements are not reflected in the loss look-up tables.

2.2 Thermal Model

A thermal description is assigned to all four of the MOSFET switches in the full bridge as well as the output diodes. These descriptions can be viewed and edited by double-clicking on the component and selecting **Edit...** from the drop-down menu of the **Thermal description** parameter. The thermal parameters were obtained from datasheets provided by Infineon, specifically for the IPW60R280P6 CoolMOS superjunction MOSFET and IDW75E60 Si power diode. For the two different device types, the thermal impedance chain representing the thermal transitions from the junction to the case are entered directly in the thermal descriptions.

Also note that the MOSFET model was customized to permit modeling multiple devices connected in series and parallel. The number of parallel or series connections can be configured in the parameter window of the MOSFETs. An equal distribution of current and voltage in both parallel- or series-

connected MOSFETs is assumed. The thermal parameters are automatically scaled to reflect the number of devices and their configuration.

Since the three heat sink components are connected together, all six devices dissipate heat into the same heat sink. A thermal resistance connects the heat sink with the temperature of the ambient air. The thermal descriptions for the MOSFETs and diodes are stored in a private thermal library in the directory `/llc_variable_frequency_resonant_converter_plecs`.

2.3 Controls

The output voltage is measured by a sensing circuit, simplified here as a transfer function (representing a low pass filter). A simplified ADC module is use to convert the measured voltage into its corresponding digital value. The output voltage measurement is compared against a DC voltage set point. The error is fed into a 2-pole, 2-zero implementation of a digital PI controller [3]. An ADC interrupt is used to trigger the interrupt service routine to run the controls (simulated here as a triggered subsystem). The controls generate a counter period set point that is then converted into a frequency set point. The frequency set point is used by the PLECS variable frequency carrier. The generated variable frequency carrier is shown in Fig. 3. The half-bridge FETs are switched with a 50% duty cycle.

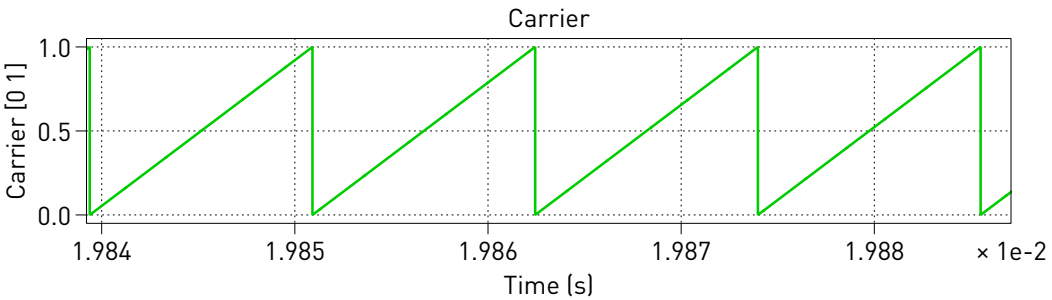

Figure 3: Carrier of the PWM generation

The LLC converter operated with variable frequency can be implemented using high fidelity ADC and PWM peripheral models, available in the PLECS Processor-in-the-Loop (PIL) component library. High fidelity peripheral modules are discussed in [4] and are used to implement the LLC converter in [5].

3 Simulation

A $200\,\mathrm{V}$ input is connected to the DC side of the full bridge. A slew rate is applied to the converter to limit the rate of change in output voltage during changes in reference voltage. Additionally, a soft start algorithm is employed to limit the rate of change in commanded voltage during startup. This is reflected on the startup transient as the output voltage incrementally ramps up. After the soft start, a voltage controller is used to control the full bridge switching frequency. The system reaches the desired $300\,\mathrm{V}$ output after $20\,\mathrm{ms}$. The plot below shows the transient simulation of the LLC converter from startup. The soft switching strategy maintains FET junction temperatures at a safe temperature range while switching at high frequency.

References

[1] R. Erickson and D. Maksimovic “Fundamentals of Power Electronics”, 2nd Edition, Springer, 2001, Chapter 19.

[2] “A More Realistic Characterization of Power MOSFET Output Capacitance Coss”, International Rectifier Application Note, AN-1001.

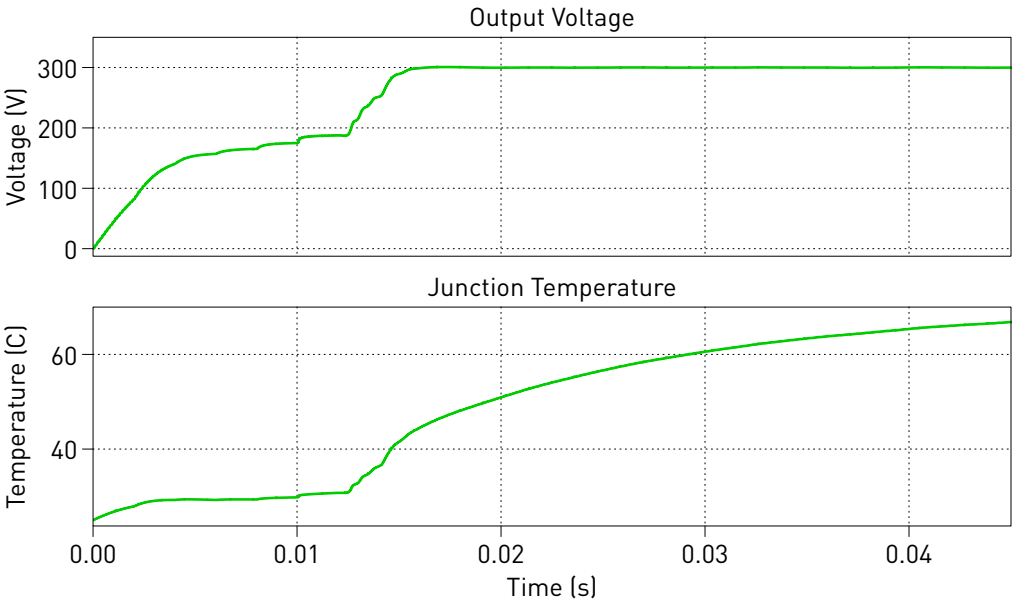

Figure 4: Simulated output voltage and junction temperature

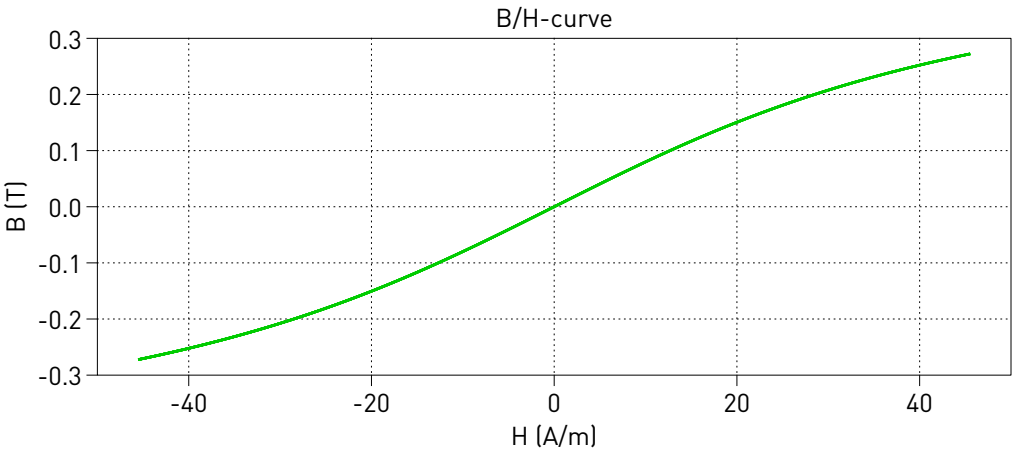

Figure 5: Simulated B-H curve of the transformer core

[3] Digital Power Control Lab “LLC Resonant Converter”, Version 1.1, Texas Instruments, Jan 2009.

[4] F. Prausse and M. Ahmed “Efficient Microcontroller Peripheral Modeling with PLECS”, Bodo’s Power Systems, July 2014 Issue, pp. 34-37.

[5] M. Ahmed and M. Luo “LLC Resonant Converter Simulation Using PLECS”, Bodo’s Power Systems, December 2014 Issue, pp. 30-33.

Revision History:

PLECS 4.3.1	First release

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PLECS Demo Model