



PLECS

DEMO MODEL

Cascaded Multilevel Inverter

Last updated in PLECS 4.3.1

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1 Overview

This demonstration illustrates a three-phase cascaded multi-cell inverter, where each cell submodule contains a full bridge. The three individual phase leg cells are implemented as a modular series-connected string of full bridges, each fed by an isolated DC source. The output voltage levels are stepped to produce $2n + 1$ levels between $-V_{dc}$ and $+V_{dc}$, where n is the number of cells. The higher number of series-connected cells both complicates the inverter hardware and its control design but can significantly reduce the harmonic distortion and therefore the need for filtering at the output. This presents an interesting tradeoff between components, cost, and performance.

The PLECS library contains power module blocks that are very useful with a modular implementation for easy scaling to create several voltage levels in multilevel converter applications, as well as having both a switched and averaged implementation. The average configuration is particularly well suited for real-time simulations with high switching frequencies, such as for hardware-in-the-loop testing. It can also increase the speed of offline simulations, because the number of internal switches is greatly reduced.

Note This model contains model initialization commands that are accessible from:

PLECS Standalone: The menu **Simulation + Simulation Parameters... + Initializations**

PLECS Blockset: Right click in the **Simulink model window + Model Properties + Callbacks + InitFcn***

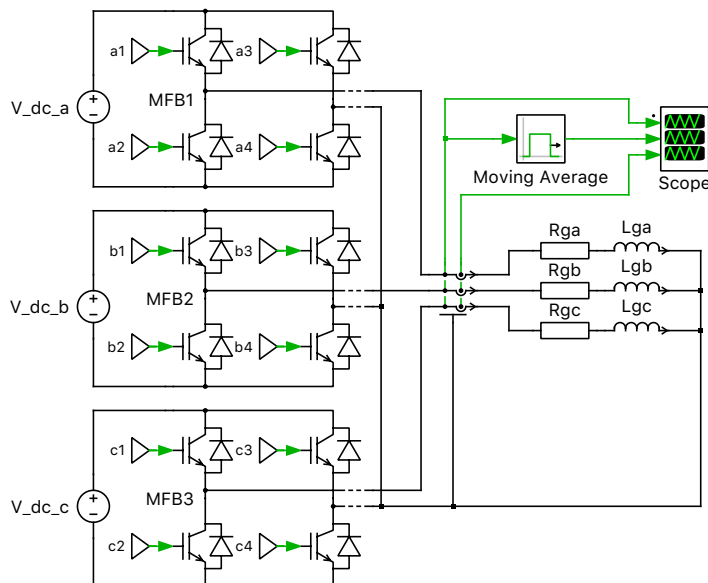


Figure 1: Top-level schematic of the model

2 Model

2.1 Power circuit

The circuit is a multilevel voltage-source inverter (VSI), with three legs, one per phase, each containing an H-bridge arrangement with IGBTs and anti-parallel diodes. Each full bridge can produce $-V_{dc}$, 0 V, $+V_{dc}$ at its output depending on the switching scheme. By cascading multiple full bridges in

series the total output voltage for each phase is the sum of the outputs of all the full bridge cells and a multilevel PWM output voltage waveform can be generated. Since the H-bridge is inherently a three-level inverter including a 0 V state, every cell added in series provides the inverter output waveform with two additional voltage levels.

In this case, the IGBT Full Bridge power module components are used. The block has two configurations: a switched configuration where ideal switches represent the semiconductors, and an averaged configuration that uses controlled voltage and current sources. The power module also has a parameter setting for the number of series-connected inverter cells. The implementation of both the power module and the controller is such that the number of cells can be configured at the top level without having to extend the model with additional wiring or components.

Each full bridge is fed by an ideal DC voltage source and this value equals the total DC bus voltage divided by the number of cascaded cells per phase. The modules are charged to the same voltage, but in reality, they could also be unbalanced if a capacitor take the place of the voltage source without an additional supply. When the modules are balanced, however, the system is very scalable. The three-phase Wye-connected RL load helps to reduce the current output ripple.

The output frequency of the grid is 50 Hz, as specified by the reference waveform of the modulator. The amplitude of the current is determined by the load and the harmonic content of the voltage waveform is influenced by the number of series-connected cells for each inverter leg.

2.2 Control

The most common modulation scheme for cascaded multilevel inverters uses phase shifted carrier pulse width modulation (PSCPWM). PSCPWM is a multicarrier modulation strategy where there is one triangular carrier per series-connected cell, and each is phase shifted by $180^\circ/n$, where 180° refers to the switching period and not the phase shift seen at the output. All of the carriers are compared to two sinusoidal reference waveforms, one for each leg of the full bridges, and these are phase shifted 180° from one another. The low side switch gating signals are complimentary to those of the high side switches so the DC bus is not shorted. A configurable dead time can also delay the switch transitions between the switch pair in each leg.

With this scheme all the modules share the workload for contributing to all voltage levels seen at the output. As expected, the more voltage levels generated by increasing the number of cascaded cells in each phase, the more closely the output voltage stepped waveform resembles a sinusoid and the less harmonic content is present.

3 Simulation

Run the simulation with the model as provided to view the signals. Observe that the output voltage is a stepped voltage in the range of ± 600 V and the number of steps is $2n$ (n = number of cells), plus an additional level at 0 V. Turn on the cursors in the PLECS Scope and set the Delta time width to the fundamental period of the grid frequency ($50 \text{ Hz} = 0.02 \text{ s}$). Then view the total harmonic distortion (THD) of the output voltage waveform. By increasing the number of cascaded cells in series using the `ncells` variable in the model initialization command window, you will notice that the THD of the voltage waveform is reduced. The number of cells in series must be six or more to reduce the THD content to $\approx 10\%$, for example.

The second plot of the Scope uses a filter block to take a moving average of the modulated output AC voltage waveform. By choosing an averaging period of the switching period (0.1 ms) we can filter out the high frequency modulations and see the 600 VAC waveform. This average will be constant regardless of the number of series-connected modules.

Now change the dead time value found in the model initialization command window to be 1% of the switching period ($0.01/f_{sw}$) and run a new simulation. The effect of this blanking time between the switch transitions in each leg is that the distortion at the output is increased and the average voltage

decreased compared to operating without any dead time. Observe the differences in THD and RMS of the voltage signals using the Scope with and without this transition delay.

Finally, increase the number of series-connected cells to 8 and run a new simulation. The simulation now takes a longer time to complete because more switching events occur as the switches are modulated with higher frequency to produce a higher number of output voltage levels. Change the power module configuration to the averaged implementation by changing `conf` to 2 in the model initialization command window and run the simulation again. This speeds up the simulation by more than two times while achieving the exact same waveforms as with the switched configuration. The effect of the speed increase using the averaged configuration becomes much more obvious if you increase the number of series-connected cells further. The averaged implementation correctly accounts for dead time so this effect can still be studied. Note that using the averaged configuration may require additional considerations such as galvanic isolation between the cells, and whether the control signals are logical or duty cycle values. See the block's documentation for more information.

4 Conclusion

Using the concept of implicit vectorization in the Power Modules from the PLECS component library allows to easily implement multilevel topologies such as a cascaded full bridges in a three-phase system. This way only one elementary full bridge cell is needed to model a modular structure with a variable number of cells. Another advantage of the Power Modules is the integrated sub-cycle average implementation that allows to study the average converter operation for controller design without any structural changes in the model.

References

- [1] B.P. McGrath and D.G. Holmes, *A comparison of multicarrier PWM strategies for cascaded and neutral point clamped multilevel inverters*, IEEE 31st Annual Power Electronics Specialists Conference, 2000, vol. 2, pp. 674-679.

Revision History:

PLECS 4.3.1 First release

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