PLECS

DEMO MODEL

Neutral-Point Clamped Converter

Last updated in PLECS 4.3.1

1 Overview

This demonstration illustrates a neutral-point clamped (NPC), three-level voltage-source inverter. The NPC topology has been adopted for high power applications as it can achieve better harmonic reduction than traditional two-level voltage source inverters and the associated control strategies help to minimize semiconductor losses. This model is designed to deliver power to a 50 Hz, 130 V_{RMS} grid from a dynamic DC source.

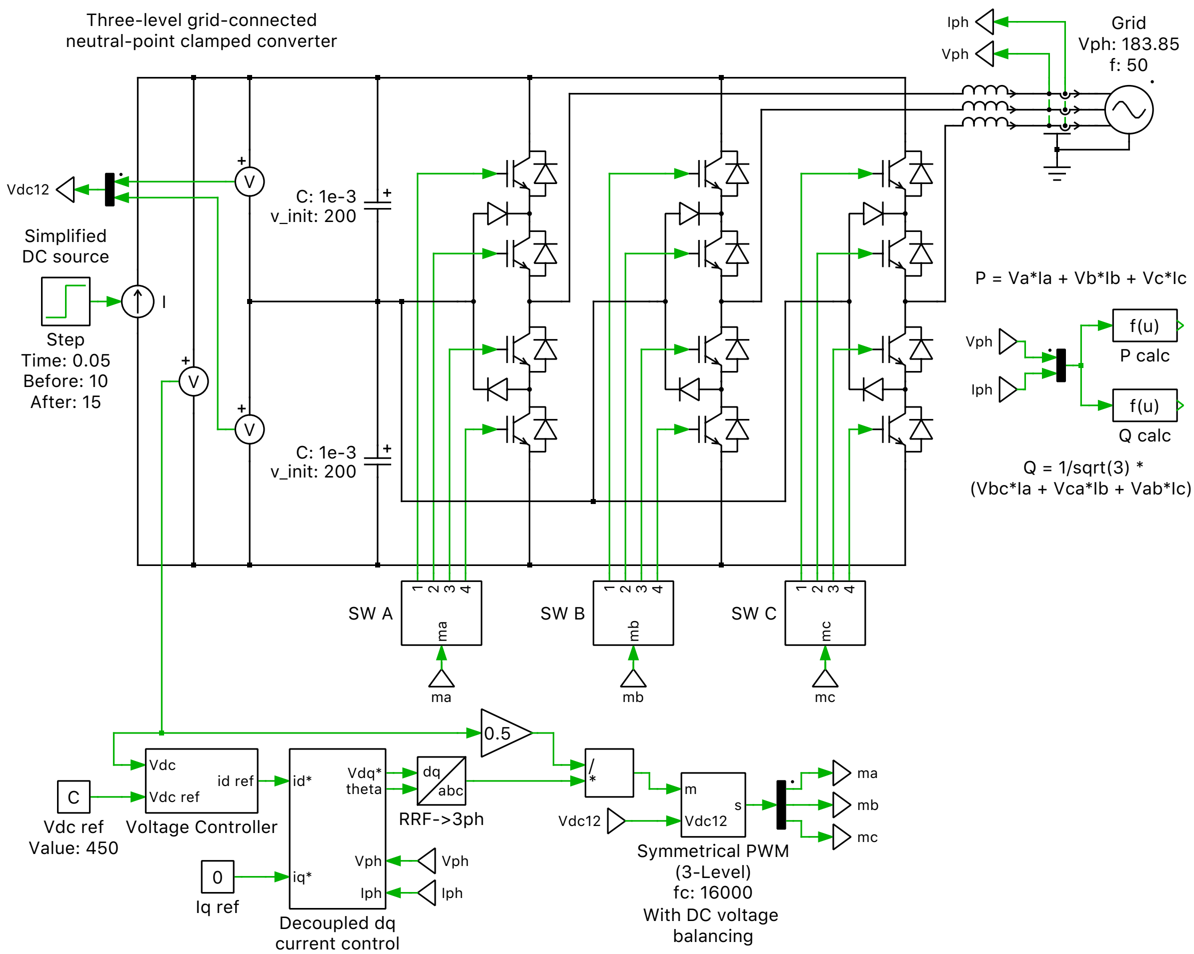

Figure 1: Neutral-point clamped converter

2 Model

2.1 Power Circuit

The circuit model is a bidirectional three-level voltage-source inverter (VSI), with three legs, one per phase, each containing two series-connected high-side switches and two series-connected low-side switches. Often, IGBTs with anti-parallel diodes are used as the switches for an NPC converter, but other two-quadrant switch configurations can also be employed. In this case, the IGBT 3-Level Half Bridge power module components are used, which each implement a single leg for an NPC converter. The power module has two configurations: a switched configuration where ideal switches represent the semiconductors, and an averaged configuration that uses controlled voltage and current sources. The averaged configuration is particularly well suited for real-time simulations with high switching frequencies, such as for hardware-in-the-loop testing.

The DC source, e.g., photovoltaic panels feeding a solar inverter, is modeled as a controlled current source. It provides $10\,\mathrm{A_{DC}}$ for the first half of the simulation and $15\,\mathrm{A_{DC}}$ for the second half of the simulation, corresponding to a sudden increase in received solar energy. This current charges the DC bus, which is split into two series-connected capacitors, with the mid-point connected to each of the three IGBT legs. Clamping diodes are placed between the capacitor mid-point and the one-quarter and three-quarter points of each leg. The mid-point of each leg is then fed to the respective phase of the AC grid via an inductor. The grid is modeled as an ideal three-phase 50 Hz, $130\,\mathrm{V_{RMS}}$ voltage source. The DC capacitors have initial voltages of $200\,\mathrm{V_{DC}}$, though the setpoint for the DC bus is $450\,\mathrm{V_{DC}}$, so they will charge up at the start of the simulation.

2.2 Controls

An outer voltage controller implemented as a PI regulator provides a current setpoint to an inner dq current controller. The voltage controller measures the DC voltage and calculates the error compared to the $450\,\mathrm{V_{DC}}$ reference value. The current controller has separate PI regulators for direct and quadrature currents that produce a Vdq reference. The AC phase voltages and currents are measured and fed to the current controller. A Phase-Locked Loop (PLL) generates the reference phase angle for the abc to dq transformations. A low pass filter is inserted into the feedback path from the Ia,b,c measurement to represent the limited bandwidth of the current sensor. Modulation indices are generated for each of the three separate modulators for the three phase legs.

3 Simulation

Run the simulation with the model as provided to view the signals and observe that the DC voltage is regulated to $450\,\mathrm{V_{DC}}$ after the transients settle. The perturbation caused by the step change in current from the PV array is regulated out in approximately 50 ms. The switching pattern clearly shows a three-level pulse train with the fundamental waveforms phase-shifted. The real and reactive power delivered to the grid can also be observed.

Revision History:

PLECS 4.3.1 First release

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