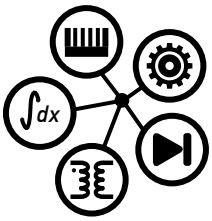

PLECS

DEMO MODEL

HVDC Transmission System with MMCs

Last updated in PLECS 4.3.1

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1 Overview

This demonstration shows a 320 kV, 200 MW high-voltage direct current (HVDC) transmission system with two modular multi-level converters (MMC) interconnecting two 110 kV high-voltage AC grids. MMCs are the prevalent type of voltage-source converter topology for HVDC applications.

At high voltages the transmission of direct current can be more efficient than alternating current. HVDC's efficiency over HVAC is a driving factor for its increasing use for power distribution. This is especially true with the integration of renewable power sources located far from the consumer, such as large-scale offshore wind generation. As a consequence new types of converters are required to interface between different electricity networks, sources, and loads.

The MMC is a bi-directional voltage source converter that interfaces the high-voltage AC and DC power systems. It comprises a positive and negative arm for each of the three phases. Each arm further contains a set of switching submodules connected in series, the number of which is chosen to achieve the desired harmonic performance and allow the use of IGBTs.

Note This model contains model initialization commands that are accessible from:

PLECS Standalone: The menu **Simulation + Simulation Parameters... + Initializations**

PLECS Blockset: Right click in the **Simulink model window + Model Properties + Callbacks + InitFcn***

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2 Model

2.1 Power Circuit

A system level overview of the model is given in Fig. 1. Both AC grids are modeled as a three-phase

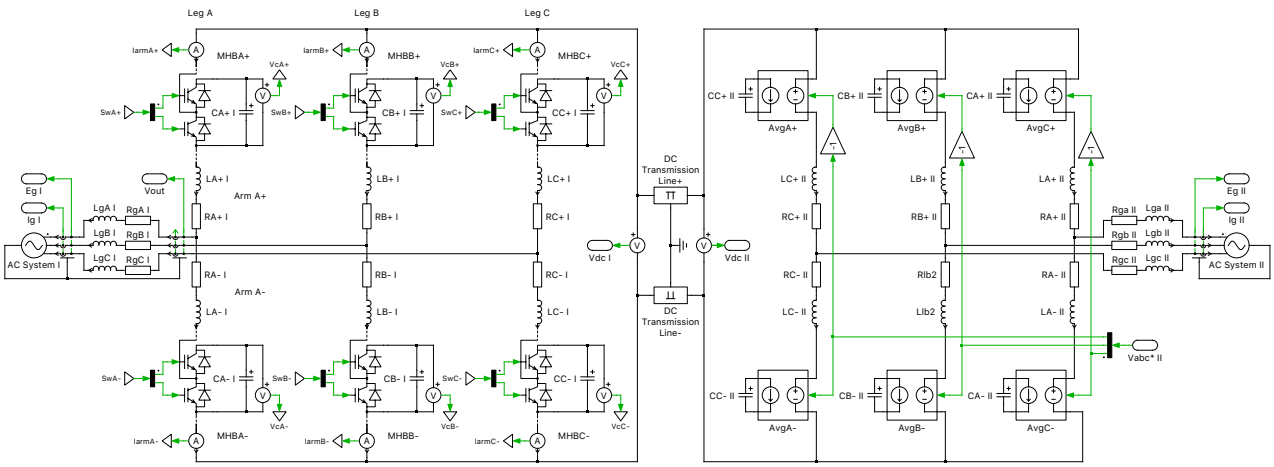

Figure 1: HVDC System with back-to-back MMCs and DC transmission line

voltage source with series impedance. The MMC connecting the AC system I and the DC system is configured to 38 submodule cells per arm. Each submodule cell is composed of one half-bridge and a DC-link capacitor. As a result, each cell has a maximum voltage of approximately 16.8 kVDC at steady state. Each single-phase pair of converter arms, together with their arm inductors, is connected to the AC system I grid. The converter arms are implemented with the "IGBT Half Bridges (Low-Side-Connected)" power module library component. This component has two configurations: a Switched

implementation where ideal switches represent the semiconductors, and an Averaged configuration that uses controlled voltage and current sources. The power module also has a parameter setting for the number of series-connected half-bridge cells. The implementation of both the power module and the controller is such that the number of cells can be configured at the top level without having to extend the model with additional wiring or components. Further, this model is configured to use the `Sub-cycle average` implementation of the power module components. Note that if fed with PWM gate signals, both configurations give exactly the same simulation result. Using the `Switched` configuration of the power modules when increasing the number of cells slows down the simulation. This is not the case for the `Sub-cycle average` configuration and therefore recommended when modeling greater numbers of cells per arm.

To make the schematic concise and organized, the IGBTs and DC capacitors are vectorized, instead of displaying 38 cells per arm in the same schematic. The Wire Multiplexer block enables a series connection of half-bridge cells for each of the six arms (2 per phase leg), resulting in only one half-bridge and DC capacitor being visible for each arm, even though 76 cells per phase leg are simulated. An explanation of this vectorization concept is provided in the demo model “STATCOM Cascaded H-Bridge Converter” in the PLECS demo models library.

The DC sides of the two AC networks are connected via two DC transmission lines, which are modeled using the PI-Section Line component. The converter arms for the MMC on the AC system II grid side are modeled as purely averaged models, similar to the `Sub-cycle average` configuration of the power modules. Equivalent voltage and current sources are employed, however, here, the switching frequency ripple effects are totally neglected. Only one DC-link capacitor is present per arm physically, which represents an average series connection of all cell capacitors. In comparison to the Averaged power module implementation, this design is simpler and increases the simulation speed.

2.2 Controls

The control scheme of the AC system I MMC can be described in two levels. The top-level control is composed of two loops. An outer loop PI controller regulates the DC transmission voltage and provides the d-axis reference for the inner current control loop. The inner current loop regulates the d- and q-axis grid currents and provides reference voltages for the MMC legs. The low-level modulator is tasked with generating the AC voltage according to the reference and at the same time active balancing of the cell voltages. A cell selection algorithm using vertically shifted carriers is implemented, ensuring that the voltage among all cells of each arm is maintained at approximately the same value.

The AC system II MMC only regulates the power flow in the form of the q-axis current. As a purely averaged model without modulated switches is used, only a top-level controller has been realized for this side. The AC voltage reference is directly fed into the six arm modules.

3 Simulation

Run the simulation with the model as provided to view the signals. The simulated AC system I converter output voltage, grid current, DC voltage, and positive cell voltages of Arm A are displayed below for the 38-level converter. The user can change the number of cells in the initialization commands to observe the effect of system complexity on simulation speed. Note that the model’s system state is initialized from the final state of a 0.3 s transient simulation. This is to skip over a large startup oscillation at the beginning of the simulation due to resonance between the arm inductor and the transmission line capacitance. In reality, a startup energizing procedure would be applied to the converter system, but is ignored here as it is not the focus of this simulation.

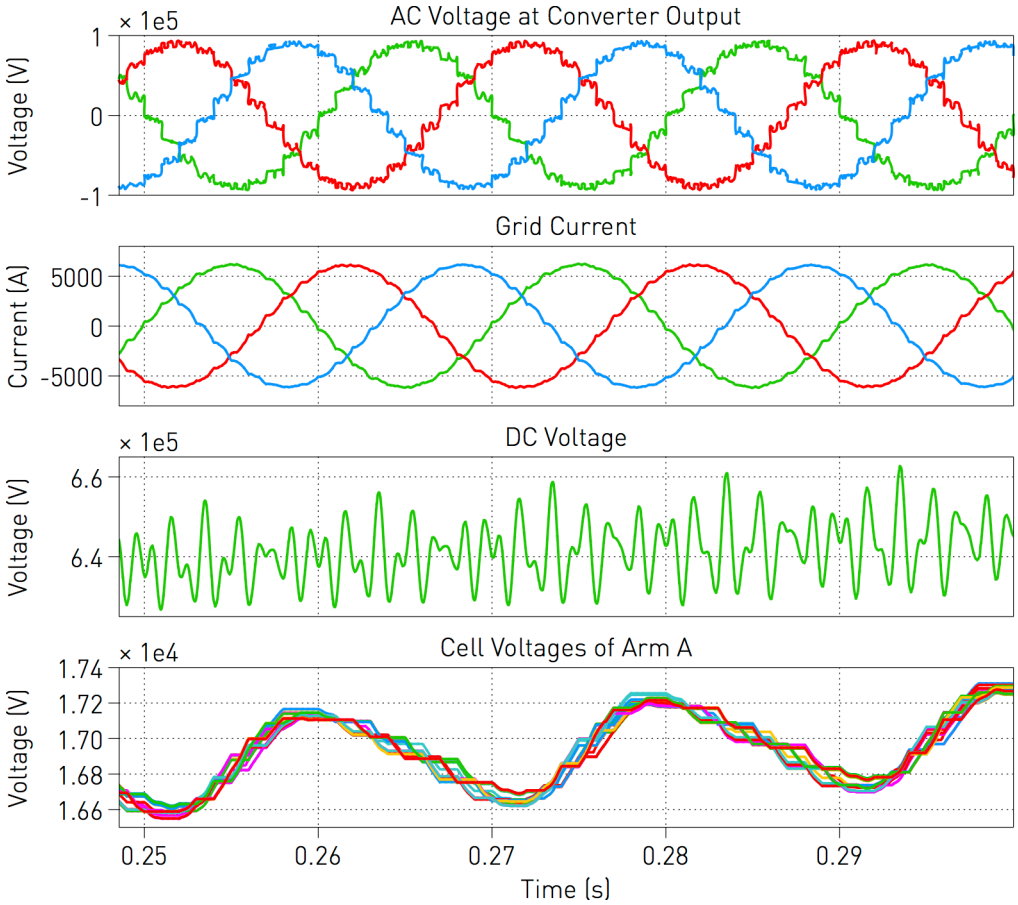

Figure 2: Simulation results

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[1] S. Rohner, S. Bernet, M. Hiller, R. Sommer, "Modulation, Losses and Semiconductor Requirements of Modular Multilevel Converters," IEEE Transactions on Industrial Electronics, Vol. 57, No. 8, August 2010.

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Revision History:

PLECS 4.3.1	First release

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PLECS Demo Model