

PLECS

*DEMO MODEL*

## Flying Capacitor DC-DC Converter

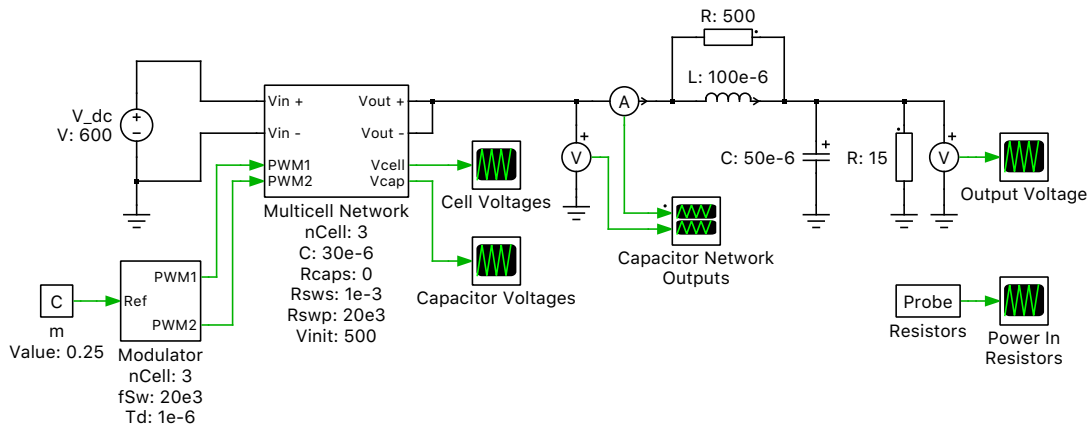
Last updated in PLECS 4.3.1

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# 1 Overview

This demonstration illustrates a flying capacitor (FC) DC/DC converter (also known as a multicell, imbricated cell or switched-capacitor converter), which is a type of multilevel converter. FC converters comprise solely switches and capacitors in the switching cell. This model is designed to step down the input voltage to an output voltage that can be configured by adjusting the duty cycle of the modulator.

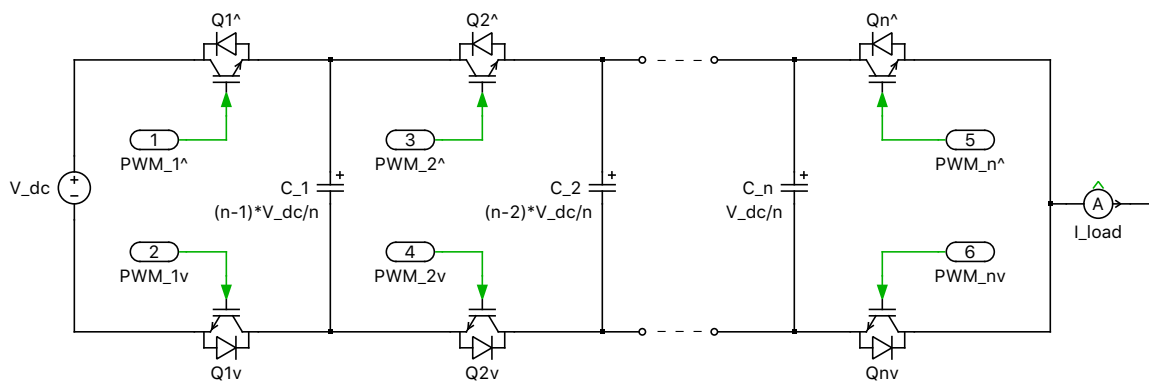


**Figure 1: Flying capacitor DC/DC converter**

## 2 Model

### 2.1 Power circuit

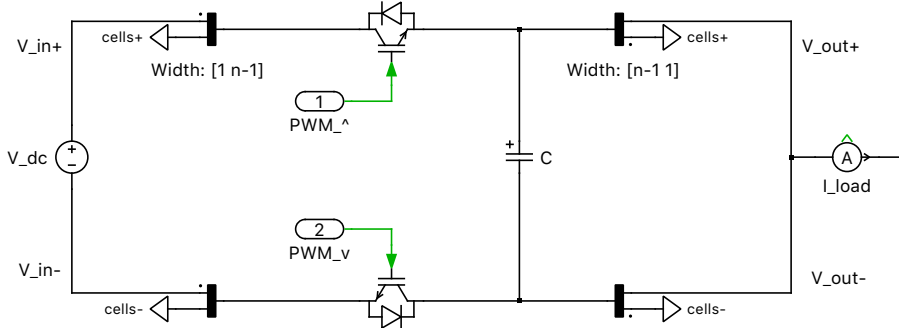
The circuit is modeled as a modular multilevel multicell network, where each cell contains two switches connected by a clamping capacitor. The switch pair and capacitors are connected in series to form a chopper circuit network. A DC voltage source powers the input and generates an AC or DC quantity at the output of the switch capacitor network, depending on the reference duty cycle of the modulator. The generic configurable-length multicell network is shown in Fig. 2.



**Figure 2: Configurable-length multicell network**

The multicell network has been implemented in PLECS using a modular subsystem concept, where a dynamically-sized chain of components is connected using wires and multiplexers. This cell implementation is depicted in Fig. 3. The input and output of the subsystem are configured as the terminals of the flying capacitor chain. The commutation cell is repeated by means of routing its output back into its input  $n - 1$  times, for a user-specified number of cells  $n$ . As shown below, the trick to this implementation is defining one of the wires in each multiplexer to have a width of  $n - 1$ . By using a wired loop,

this creates a chain with the components in between the multiplexers (a switch pair and clamping capacitor) being replicated in a series-connected fashion  $n$  times.



**Figure 3: Cell implementation of flying capacitor DC/DC converter**

The balanced chopped capacitor voltage levels are  $0, V_{dc}/n, 2 \cdot V_{dc}/n, \dots, (n-1)V_{dc}/n$ .

Since the input is 600 VDC and  $n = 3$ , the capacitor voltage levels are 0, 200, and 400 VDC. The output of the capacitor network has significant ripple and needs to be filtered before the load. An LC low pass filter is used for this purpose. A voltage booster is also included in parallel to the inductor, which helps to speed up the balancing of the system during transients [1].

## 2.2 Control

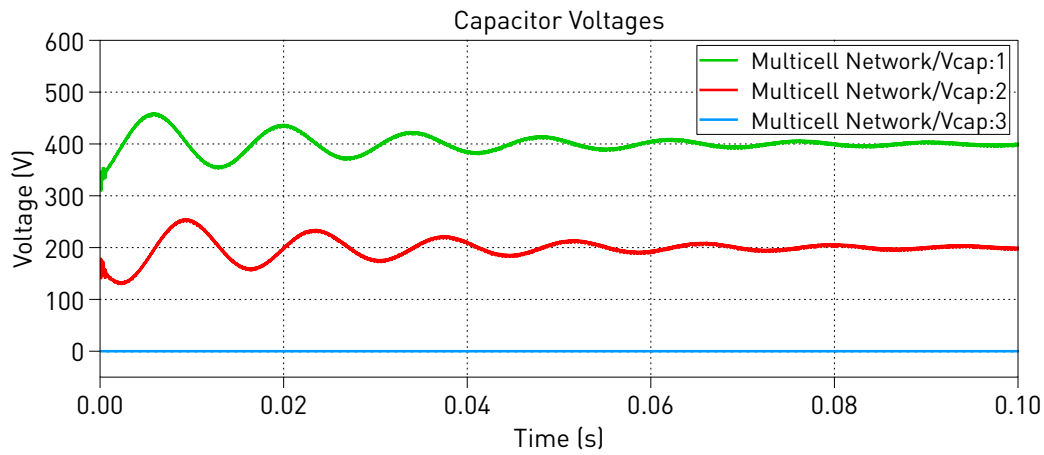
The modulation scheme is a phase shifted carrier pulse-width modulation (PSCPWM) technique using a fixed duty cycle. There are  $n$  triangular carriers, each shifted from the previous one by  $2\pi/n$ . The controller provides two pulse-width modulated signals that gate the upper and lower IGBTs with the same duty cycle, but shifted by  $180^\circ$ . A dead time is included to delay the turn-on between switch commutation for each switch pair. The converter doesn't require closed-loop control because the capacitors themselves will self-balance as each commutation cell has equal duty cycles and  $2\pi/n$  phase shifts, as discussed in [2]. Any changes to the DC input or having unbalanced initial capacitor voltages will produce a transient, but the system will settle to a well-defined steady-state operating point without feedback regulation.

## 3 Simulation

Run the simulation with the model as provided to view the signals and verify that the load settles at  $V_{dc} \cdot D = 600 \text{ V} \cdot 0.25$ , or approximately 150 VDC. In fact, the voltage at the load is slightly less due to losses in the non-idealities of the switches and at the output network. The output voltage can be adjusted by changing the duty cycle reference constant that is fed into the Modulator subsystem. Also, the number of cells in the network can be changed, but be sure to set the same number for this parameter in both the circuit subsystem and controller subsystem. The self-balancing nature of the capacitor network is shown with the transient behavior of the waveforms in the "Cell Voltages" and "Capacitor Voltages" scopes. Capacitor voltages at different cell output are depicted in Fig. 4. By providing an initial voltage to the capacitors (500 VDC) that is different than the DC bus (600 VDC), the capacitor voltages will migrate towards stacked DC levels of  $V_{dc}/n$  and the cell voltages will all balance each other at  $V_{dc}/n = 200$  VDC.

## References

- [1] T. A. Meynard, H. Foch, P. Thomas, et al, "Multicell converters: Basic concepts and industry applications", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 955-964, Oct. 2002.



**Figure 4: Simulation result of capacitor voltages at different cell output**

- [2] R. H. Wilkinson, T. A. Meynard, and H. du T. Mouton, "Natural balance of multicell converters: The general case", *IEEE Transactions on Power Electronics*, vol. 21, pp. 1658-1666, Nov. 2006.

## Revision History:

PLECS 4.3.1      First release

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